

**KM424C257****CMOS VIDEO RAM***256Kx4 Bit CMOS Video RAM***FEATURES**

- **Dual port Architecture**  
256K x 4 bits RAM port  
512 x 4 bits SAM port
- **Performance**

Parameter \ Speed	-6	-7	-8
RAM access time (t <sub>RAC</sub> )	60ns	70ns	80ns
RAM access time (t <sub>CAC</sub> )	20ns	20ns	20ns
RAM cycle time (t <sub>RC</sub> )	110ns	130ns	150ns
RAM page mode cycle (t <sub>PC</sub> )	40ns	45ns	50ns
SAM access time (t <sub>SCA</sub> )	18ns	20ns	20ns
SAM cycle time (t <sub>SCC</sub> )	20ns	25ns	25ns
RAM active current	90mA	85mA	80mA
SAM active current	50mA	45mA	40mA

- **Fast Page Mode**
- **RAM Read, Write, Read-Modify-Write**
- **Serial Read and Serial Write**
- **Read, Real Time Read and Split Read Transfer (RAM→SAM)**
- **Write, Split Write Transfer with Masking operation (New Mask)**
- **Block Write, Flash Write and Write per bit with Masking operation (New Mask)**
- **CAS-before-RAS, RAS-only and Hidden Refresh**
- **Common Data I/O Using three state RAM Output Control**
- **All Inputs and outputs TTL compatible**
- **Refresh: 512 Cycle/8ms**  
Single +5V ± 10% Supply Voltage
- **Plastic 28-PIN 400 mil SOJ and ZIP**

**GENERAL DESCRIPTION**

The Samsung KM424C257 is a CMOS 256Kx4 bit Dual Port DRAM. It consists of a 256Kx4 dynamic random access memory (RAM) port and 512x4 static serial access memory (SAM) port. The RAM and SAM ports operate asynchronously except during data transfer between the ports.

The RAM array consists of 512 bit rows of 2048 bits. It operates like a conventional 256Kx4 CMOS DRAM. The RAM port has a write per bit mask capability.

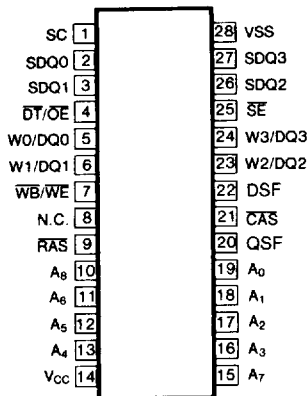
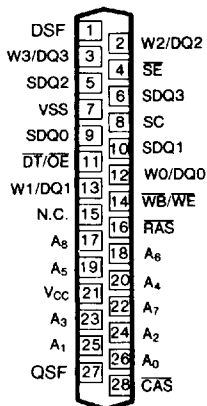
The SAM port consists of four 512 bit high speed shift registers that are connected to the RAM array through a 2048 bit data transfer gate. The SAM port has serial read and write capabilities.

Data may be internally transferred bi-directionally between the RAM and SAM ports using read or write transfers.

Refresh is accomplished by familiar DRAM refresh modes. The KM424C257 supports RAS-only, Hidden, and CAS-before-RAS refresh for the RAM port. The SAM port does not require refresh.

All inputs and I/O's are TTL level compatible. All address lines and Data Inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

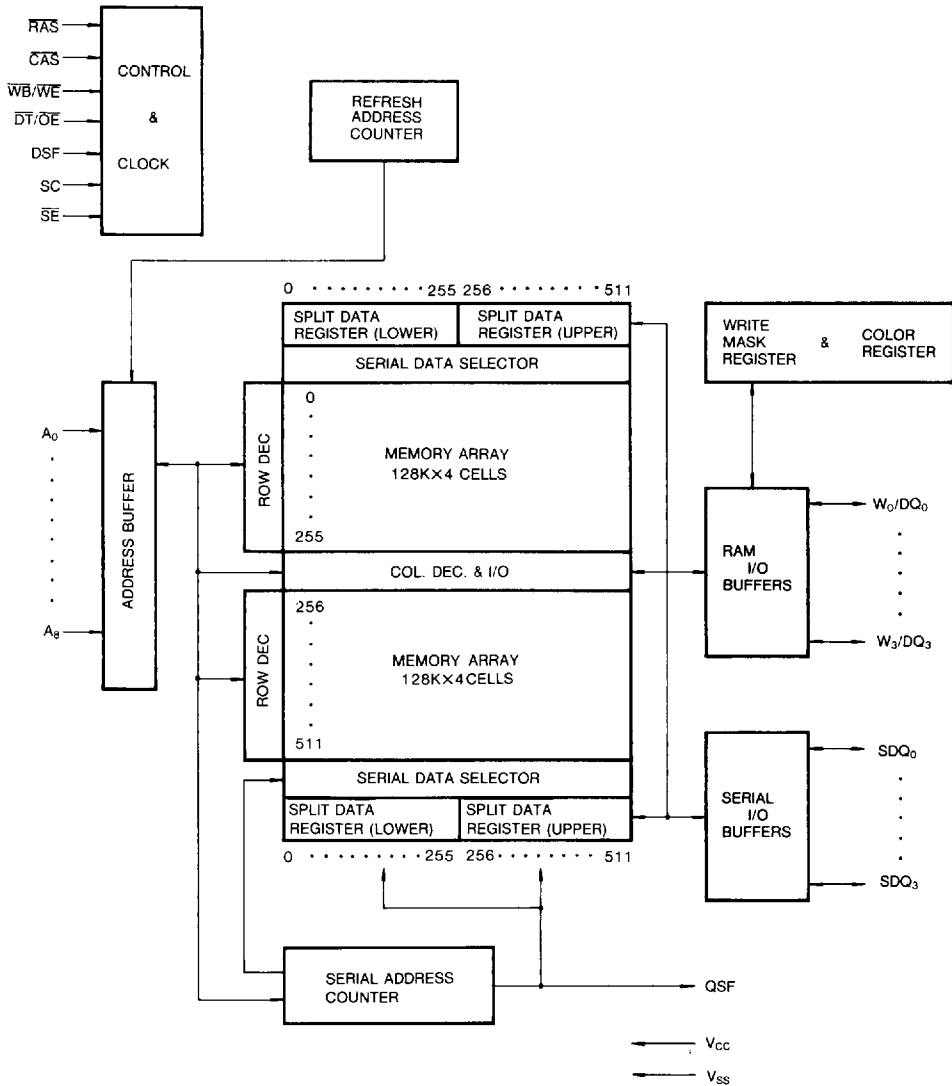
Pin Name	Pin Function
SC	Serial Clock
SDQ <sub>0</sub> -SDQ <sub>3</sub>	Serial Data Input / Output
$\overline{DT/OE}$	Data Transfer / Output Enable
$\overline{WB/WE}$	Write Per Bit / Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
W <sub>0</sub> /DQ <sub>0</sub> -W <sub>3</sub> /DQ <sub>3</sub>	Data Write Mask / Input / Output
$\overline{SE}$	Serial Enable
A <sub>0</sub> -A <sub>8</sub>	Address Inputs
V <sub>CC</sub>	Power (+5)
V <sub>SS</sub>	Ground
N.C.	No Connection
DSF	Special Function Control
QSF	Special Flag Output

**KM424C257****CMOS VIDEO RAM****PIN CONFIGURATION** (Top Views)**28 Pin 400 mil SOJ****28 Pin 400 mil ZIP**

**KM424C257**

**CMOS VIDEO RAM**

**FUNCTIONAL BLOCK DIAGRAM**



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**KM424C257****CMOS VIDEO RAM****ABSOLUTE MAXIMUM RATINGS\***

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-1 to +7.0	V
Voltage on $V_{CC}$ Supply Relative to $V_{SS}$	$V_{CC}$	-1 to +7.0	V
Storage Temperature	$T_{stg}$	-55 to +150	°C
Power Dissipation	$P_D$	1	W
Short Circuit Output Current	$I_{OS}$	50	mA

\* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS** (Voltage reference to  $V_{SS}$ ,  $T_A=0$  to  $70^\circ\text{C}$ )

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
Ground	$V_{SS}$	0	0	0	V
Input High Voltage	$V_{IH}$	2.4	—	6.5	V
Input Low Voltage	$V_{IL}$	-1.0	—	0.8	V

**INPUT/OUTPUT CURRENT** (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current (Any Input $0 \leq V_{IN} \leq 6.5\text{V}$ , all other pins not under test=0 volts.)	$I_{IL}$	-10	10	$\mu\text{A}$
Output Leakage Current (Data out is disabled, $0\text{V} \leq V_{OUT} \leq 5.5\text{V}$ )	$I_{OL}$	-10	10	$\mu\text{A}$
Output High Voltage Level (RAM $I_{OH} = -5\text{mA}$ , SAM $I_{OH} = -2\text{mA}$ )	$V_{OH}$	2.4	—	V
Output Low Voltage Level (RAM $I_{OL} = 4.2\text{mA}$ , SAM $I_{OL} = 2\text{mA}$ )	$V_{OL}$	—	0.4	V

**CAPACITANCE** ( $t_A=25^\circ\text{C}$ )

Item	Symbol	Min	Max	Unit
Input Capacitance ( $A_0-A_8$ )	$C_{IN1}$	2	6	pF
Input Capacitance ( $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WB/WE}$ , $\overline{DT/OE}$ , $\overline{SE}$ , $SC$ , $DSF$ )	$C_{IN2}$	2	7	pF
Input/Output Capacitance ( $W_0/DQ_0-W_3/DQ_3$ )	$C_{DQ}$	2	7	pF
Input/Output Capacitance ( $SDQ_0-SDQ_3$ )	$C_{SDQ}$	2	7	pF
Output Capacitance ( $QSF$ )	$C_{QSF}$	2	7	pF

**KM424C257****CMOS VIDEO RAM****DC AND OPERATING CHARACTERISTICS**

(Recommended operating conditions unless otherwise noted)

Parameter(RAM Port)	SAM Port	Symbol	KM424C257			Unit
			-6	-7	-8	
Operating Current*1 ( $\overline{RAS}$ and $\overline{CAS}$ Cycling @ $t_{RC}=\text{min.}$ )	Standby	I <sub>CC1</sub>	90	85	80	mA
	Active	I <sub>CC1A</sub>	140	130	120	mA
Standby Current*1 ( $\overline{RAS}=\overline{CAS}=\overline{DT}/\overline{OE}=\overline{WB}/\overline{WE}=V_{IH}, DSF=V_{IL}$ )	Standby	I <sub>CC2</sub>	5	5	5	mA
	Active	I <sub>CC2A</sub>	50	45	40	mA
$\overline{RAS}$ Only Refresh Current*1 ( $\overline{CAS}=V_{IH}$ , $\overline{RAS}$ Cycling @ $t_{RC}=\text{min.}$ )	Standby	I <sub>CC3</sub>	90	85	80	mA
	Active	I <sub>CC3A</sub>	140	130	120	mA
Fast Page Mode Current*1 ( $\overline{RAS}=V_{IL}$ , $\overline{CAS}$ Cycling @ $t_{PC}=\text{min.}$ )	Standby	I <sub>CC4</sub>	70	65	60	mA
	Active	I <sub>CC4A</sub>	120	110	100	mA
$\overline{CAS}$ -Before- $\overline{RAS}$ Refresh Current*1 ( $\overline{RAS}$ and $\overline{CAS}$ Cycling @ $t_{RC}=\text{min.}$ )	Standby	I <sub>CC5</sub>	90	85	80	mA
	Active	I <sub>CC5A</sub>	140	130	120	mA
Data Transfer Current*1 ( $\overline{RAS}$ and $\overline{CAS}$ Cycling @ $t_{RC}=\text{min.}$ )	Standby	I <sub>CC6</sub>	120	115	110	mA
	Active	I <sub>CC6A</sub>	170	160	150	mA
Flash Write Cycle ( $\overline{RAS}$ and $\overline{CAS}$ Cycling @ $t_{RC}=\text{min.}$ )	Standby	I <sub>CC7</sub>	90	85	80	mA
	Active	I <sub>CC7A</sub>	140	130	120	mA
Block Write Cycle ( $\overline{RAS}$ and $\overline{CAS}$ Cycling @ $t_{RC}=\text{min.}$ )	Standby	I <sub>CC8</sub>	100	95	90	mA
	Active	I <sub>CC8A</sub>	150	140	130	mA
Color Register Load or Read Cycle ( $\overline{RAS}$ and $\overline{CAS}$ Cycling @ $t_{RC}=\text{min.}$ )	Standby	I <sub>CC9</sub>	90	85	80	mA
	Active	I <sub>CC9A</sub>	140	130	120	mA

NOTE\*1: Real values are dependent on output loading and cycle rates. Specified values are obtained with the output open, I<sub>CC</sub> is Specified as average current.

In I<sub>CC1</sub>, I<sub>CC3</sub>, address transition should be changed only once while  $\overline{RAS}=V_{IL}$ .

In I<sub>CC4</sub>, address transition should be changed only once while  $\overline{CAS}=V_{IH}$ .

## KM424C257

## CMOS VIDEO RAM

AC CHARACTERISTICS ( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ,  $V_{CC}=5.0\text{V} \pm 10\%$ , see notes 1,2)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	110		130		150		ns	
Read-modify-write cycle time	trwc	155		175		20		ns	
Fast page mode cycle time	tpc	40		45		50		ns	
Fast page mode read-modify-write	tprow	80		85		90		ns	
Access time from $\overline{\text{RAS}}$	trac		60		70		80	ns	3,4
Access time from $\overline{\text{CAS}}$	tcac		20		20		20	ns	4
Access time from column address	tAA		30		35		40	ns	3,11
Access time from $\overline{\text{CAS}}$ precharge	tCPA		35		40		45	ns	3
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	3		3		3		ns	3
Output buffer turn-off delay	toff	0	15	0	15	0	15	ns	7
Transition time(rise and fall)	tt	3	50	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	trp	40		50		60		ns	
$\overline{\text{RAS}}$ pulse width	trasp	60	10K	70	10K	80	10K	ns	
$\overline{\text{RAS}}$ pulse width(fast page mode)	trasp	60	100K	70	100K	80	100K	ns	
$\overline{\text{RAS}}$ hold time	trsh	20		20		20		ns	
$\overline{\text{CAS}}$ hold time	tCSH	60		70		80		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	20	10K	20	10K	20	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	trcd	20	40	20	50	25	60	ns	5,6
$\overline{\text{RAS}}$ to column address delay time	trAD	15	30	15	35	20	40	ns	11
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time	tCPN	10		10		10		ns	
$\overline{\text{CAS}}$ precharge time(fast page mode)	tCP	10		10		10		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		15		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	15		15		15		ns	
Column address hold referenced to $\overline{\text{RAS}}$	tAR	50		55		60		ns	
Column address to $\overline{\text{RAS}}$ lead time	trAL	30		35		40		ns	
Read command set-up time	trCS	0		0		0		ns	
Read command hold referenced to $\overline{\text{CAS}}$	trCH	0		0		0		ns	9
Read command hold referenced to $\overline{\text{RAS}}$	trRH	0		0		0		ns	9
Write command hold time	twCH	15		15		15		ns	
Write command hold referenced to $\overline{\text{RAS}}$	twCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	trWL	15		15		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tcWL	15		15		20		ns	

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## CMOS VIDEO RAM

## AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	15		15		15		ns	10
Data hold referenced to $\overline{\text{RAS}}$	tDHR	45		55		60		ns	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay	tCWD	40		45		45		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay	tRWD	85		95		105		ns	8
Column address to $\overline{\text{WE}}$ delay time	tAWD	55		60		65		ns	8
$\overline{\text{CAS}}$ setup time(C-B-R refresh)	tCSR	10		10		10		ns	
$\overline{\text{CAS}}$ hold time(C-B-R refresh)	tCHR	10		10		10		ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	tRPC	10		10		10		ns	
$\overline{\text{RAS}}$ hold time referenced to $\overline{\text{OE}}$	tROH	15		20		20		ns	7
Access time from output enable	tOEA		20		20		20	ns	
Output enable to data input delay	tOED	15		15		15		ns	
Output buffer turn-off delay time from $\overline{\text{OE}}$	tOEZ	0	15	0	15	0	15	ns	
Output enable command hold time	tOEH	15		15		15		ns	
Data to $\overline{\text{CAS}}$ delay	tDZC	0		0		0		ns	
Data to output enable delay	tDZO	0		0		0		ns	
Refresh period(512 cycle)	tREF		8		8		8	ms	
$\overline{\text{WB}}$ set-up time	tWSR	0		0		0		ns	
$\overline{\text{WB}}$ hold time	tRWH	10		10		15		ns	
DSF set-up time referenced to $\overline{\text{RAS}}$ ( I )	tFSR	0		0		0		ns	
DSF hold time referenced to $\overline{\text{RAS}}$ ( I )	tFHR	45		55		60		ns	
DSF hold time referenced to $\overline{\text{RAS}}$ ( II )	tRFH	10		10		15		ns	
DSF set-up time referenced to $\overline{\text{CAS}}$	tFSC	0		0		0		ns	
DSF hold time referenced to $\overline{\text{CAS}}$	tCFH	10		15		15		ns	
Write per bit mask data set-up	tMS	0		0		0		ns	
Write per bit mask data hold	tMH	10		10		15		ns	
$\overline{\text{DT}}$ high set-up time	tTHS	0		0		0		ns	
$\overline{\text{DT}}$ high hold time	tTHH	10		10		15		ns	
$\overline{\text{DT}}$ high set-up time	tTLS	0		0		0		ns	
$\overline{\text{DT}}$ low hold time	tTLH	10		10		15		ns	
$\overline{\text{DT}}$ low hold ref to $\overline{\text{RAS}}$ (real time read transfer)	tRTH	50		60		65		ns	
$\overline{\text{DT}}$ low hold ref to $\overline{\text{CAS}}$ (real time read transfer)	tCTH	15		20		25		ns	
$\overline{\text{DT}}$ low hold ref to col.addr.(real time read transfer)	tATH	20		25		30		ns	
$\overline{\text{SE}}$ set-up referenced to $\overline{\text{RAS}}$	tESR	0		0		0		ns	
$\overline{\text{SE}}$ hold time referenced to $\overline{\text{RAS}}$	tREH	10		10		15		ns	

## KM424C257

## CMOS VIDEO RAM

## AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{DT}$ to $\overline{RAS}$ precharge time	tTRP	40		50		60		ns	
$\overline{DT}$ precharge time	tTp	20		20		25		ns	
$\overline{RAS}$ to first SC delay (read transfer)	tRSD	60		70		80		ns	
$\overline{CAS}$ to first SC delay (read transfer)	tCSD	25		30		35		ns	
Col.Addr.to first SC delay (read transfer)	tASD	35		40		40		ns	
Last SC to $\overline{DT}$ lead time	tTSL	5		5		5		ns	
$\overline{DT}$ to first SC delay time (read transfer)	tRSD	10		10		15		ns	
Last SC to $\overline{RAS}$ set-up time (serial input)	tSRS	30		30		30		ns	
$\overline{RAS}$ to first SC delay time (serial input)	tSRD	20		20		25		ns	
$\overline{RAS}$ to serial input delay time	tSDD	30		40		50		ns	
Serial output buffer turn-off delay from $\overline{RAS}$ (pseudo write transfer)	tSDZ	10	30	10	30	10	35	ns	7
Serial Input to first SC delay time	tSZS	0		0		0		ns	
SC cycle time	tSCC	20		25		25		ns	12
SC pulse width (SC high time)	tSC	6		7		7		ns	
SC precharge (SC low time)	tSCP	6		7		7		ns	
Access time from SC	tSCA		18		20		20	ns	4
Serial output hold time from SC	tSOH	5		5		5		ns	
Serial input set-up time	tSDS	0		0		0		ns	
Serial input hold time	tSDH	10		15		15		ns	
Access time from $\overline{SE}$	tSEA		15		20		20	ns	4
$\overline{SE}$ pulse width	tSE	20		20		25		ns	
$\overline{SE}$ precharge time	tSEP	20		20		25		ns	
Serial output turn-off from $\overline{SE}$	tSEZ	0	15	0	15	0	15	ns	7
Serial input to $\overline{SE}$ delay time	tSZE	0		0		0		ns	
Serial write enable set-up time	tSWS	5		5		5		ns	
Serial write enable hold time	tSWH	10		15		15		ns	
Serial write disable set-up time	tSWIS	5		5		5		ns	
Serial write disable hold time	tSWIH	15		15		15		ns	
Split transfer set-up time	tSTS	25		25		25		ns	
Split transfer hold time	tSTH	25		25		25		ns	
SC-QSF delay time	tSQD		25		25		25	ns	
$\overline{DT}$ -QSF delay time	tTQD		25		25		25	ns	
$\overline{CAS}$ -QSF delay time	tCQD		30		35		40	ns	
$\overline{RAS}$ -QSF delay time	tRQD		60		70		80	ns	

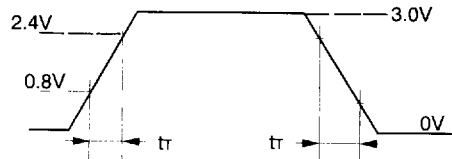


## KM424C257

## CMOS VIDEO RAM

## NOTES

1. An initial pause of 200 $\mu$ s is required after power-up followed by any 8 RAS, 8 SC cycles before proper device operation is achieved. If the internal refresh counter is used a minimum of 8 CAS-before-RAS initialization cycles are required instead of 8 RAS cycles.
2.  $V_{IH(min)}$  and  $V_{IL(max)}$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH(min)}$  and  $V_{IL(max)}$ , and are assumed to be 5ns for all inputs. Inputs signal transition from 0 to 3V for AC Testing.
3. RAM port outputs are measured with a load equivalent to 2 TTL loads and 100pF. Dout comparator level:  $V_{OH}/V_{OL}=2.0/0.8V$
4. SAM port outputs are measured with a load equivalent to 1 TTL loads and 50pF. Dout comparator level:  $V_{OH}/V_{OL}=2.0/0.8V$ .
5. Operation within the  $t_{RCD(max)}$  limit insures that  $t_{RAC(max)}$  can be met.  $t_{RCD(max)}$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD(max)}$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
6. Assumes that  $t_{RCD} \geq t_{RCD(max)}$ .
7. The parameters,  $t_{OFF(max)}$ ,  $t_{OEZ(max)}$ ,  $t_{SDZ(max)}$  and  $t_{SEZ(max)}$ , define the time at which the output achieves the open circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
8.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS(min)}$  the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If  $t_{CWD} \geq t_{CWD(min)}$  and  $t_{RWD} \geq t_{RWD(min)}$  and  $t_{AWD} \geq t_{AWD(min)}$ , then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either  $t_{RCH}$  or  $t_{RAH}$  must be satisfied for a read cycle.
10. These parameters are referenced to the  $\overline{CAS}$  leading edge in early write cycles and to the  $\overline{WE}$  leading edge in read-write cycles.
11. Operation within the  $t_{RAD(max)}$  limit insures that  $t_{RCD(max)}$  can be met.  $t_{RAD(max)}$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD(max)}$  limit, then access time is controlled by  $t_{AA}$ .
12. Assume  $t_r=3ns$
13. Recommended operating input condition.



Input pulse levels are from 0.0V to 3.0Volts.

All timing measurements are referenced from  $V_{IL(max)}$  and  $V_{IH(min)}$  with transition time = 3.0ns

**KM424C257****CMOS VIDEO RAM****DEVICE OPERATION**

The KM424C257 contains 1,048,576 memory locations. Eighteen address bits are required to address a particular 4-bit word in the memory array. Since the KM424C257 has only 0 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ( $\overline{RAS}$ ), the column address strobe ( $\overline{CAS}$ ) and the valid row and column address inputs.

Operation of the KM424C257 begins by strobing in a valid row address with  $\overline{RAS}$  while  $\overline{CAS}$  remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by  $\overline{CAS}$ . This is the beginning of any KM424C257 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both  $\overline{RAS}$  and  $\overline{CAS}$  have returned to the high state. Another cycle can be initiated after  $\overline{RAS}$  remains high long enough to satisfy the  $\overline{RAS}$  precharge time ( $t_{RP}$ ) requirement.

 **$\overline{RAS}$  and  $\overline{CAS}$  Timing**

The minimum  $\overline{RAS}$  and  $\overline{CAS}$  pulse widths are specified by  $t_{RAS(min)}$  and  $t_{CAS(min)}$  respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing  $\overline{RAS}$  low, it must not be aborted prior to satisfying the minimum  $\overline{RAS}$  and  $\overline{CAS}$  pulse widths. In addition, a new cycle must not begin until the minimum  $\overline{RAS}$  precharge time,  $t_{RP}$ , has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM424C257 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

**Read**

A read cycle is achieved by maintaining  $\overline{WB}/\overline{WE}$  high during a  $\overline{RAS}/\overline{CAS}$  cycle. The access time is normally specified with respect to the falling edge of  $\overline{RAS}$ . But the access time also depends on the falling edge of  $\overline{CAS}$  and on the valid column address transition. If  $\overline{CAS}$  goes low

before  $t_{RCO(max)}$  and if the column address is valid before  $t_{RAD(max)}$  then the access time to valid data is specified by  $t_{RAC(min)}$ . However, if  $\overline{CAS}$  goes low after  $t_{RCO(max)}$  or if the column address becomes valid after  $t_{RAD(max)}$ , access is specified by  $t_{CAC}$  or  $t_{AA}$ .

The KM424C257 has common data I/O pins. The  $\overline{DT}/\overline{OE}$  has been provided so the output buffer can be precisely controlled. For data to appear at the outputs,  $\overline{DT}/\overline{OE}$  must be low for the period of time defined by  $t_{OEA}$ .

**Write**

The KM424C257 can perform early write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between  $\overline{WB}/\overline{WE}$ ,  $\overline{DT}/\overline{OE}$  and  $\overline{CAS}$ . In any type of write cycle, Data-in must be valid at or before the falling edge of  $\overline{WB}/\overline{WE}$ , whichever is later.

**Fast Page Mode**


Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while  $\overline{RAS}$  is kept low to maintain the row address,  $\overline{CAS}$  is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

**Write-Per-Bit**

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When  $\overline{WB}/\overline{WE}$  is held 'low' at the falling edge of  $\overline{RAS}$ , during a random access operation, the write-mask is enabled. At the same time, the mask data on the  $W_i/DQ_i$  pins is latched onto the write-mask register ( $WM1$ ). When a '0' is sensed on any of the  $W_i/DQ_i$  pins, their corresponding write circuits are disabled and new data will not be written.

When a '1' is sensed on any of the  $W_i/DQ_i$  pins, their corresponding write circuits will remain enabled so that new data is written. The write mask data is valid for only one cycle the truth table of the write-per-bit function are shown in Table 1.

**Table 1. Truth table for write-per-bit function**

$\overline{RAS}$	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$W_i/DQ_i$	FUNCTION
	H	H	H	*	WRITE ENABLE
	H	H	L	1	WRITE ENABLE
	H	H	L	0	INHIBIT WRITE

# KM424C257

# CMOS VIDEO RAM

## DEVICE OPERATION (Continued)

### Block Write

A block write cycle is performed by holding  $\overline{\text{CAS}}$ ,  $\overline{\text{DT}}/\overline{\text{OE}}$  "high" and DSF "Low" at the falling edge of  $\overline{\text{RAS}}$  and by holding DSF "high" at the falling edge of  $\overline{\text{CAS}}$ . The state of the  $\overline{\text{WB}}/\overline{\text{WE}}$  at the falling edge of  $\overline{\text{RAS}}$  determines whether or not the I/O data mask is enabled as write per bit function. At the falling edge of  $\overline{\text{CAS}}$ , the starting column address pointer and column mask data must be provided. During a block write cycle, the 2 least significant column address ( $A_0$  and  $A_1$ ) are internally controlled and only the seven most significant column address ( $A_2$ - $A_8$ ) are latched at the falling edge of  $\overline{\text{CAS}}$ .

### Flash Write

Flash write is mainly used for fast clear operations in frame buffer applications. A flash write cycle is performed by holding  $\overline{\text{CAS}}$  "high",  $\overline{\text{WB}}/\overline{\text{WE}}$  "Low" and DSF "high" at the falling edge of  $\overline{\text{RAS}}$ . The mask data must also be provided on the  $\overline{\text{W}}/\overline{\text{DQ}}_i$  lines at the falling edge of  $\overline{\text{RAS}}$  in order to enable the flash write operation for selected I/O blocks.

### Data Output

The KM424C257 has a three state output buffers which are controlled by  $\overline{\text{CAS}}$  and  $\overline{\text{DT}}/\overline{\text{OE}}$ . When either  $\overline{\text{CAS}}$  or  $\overline{\text{DT}}/\overline{\text{OE}}$  is high ( $V_{IH}$ ) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by  $t_{OL}$  after the falling edge of  $\overline{\text{CAS}}$ . Invalid data may be present at the output during the time after  $t_{OL}$  and before the valid data appears at the output. The timing parameters  $t_{CAC}$ ,  $t_{RAC}$  and  $t_{AA}$  specify when the valid data will be present at the output. The valid data remains at the output until  $\overline{\text{CAS}}$  returns high. This is true even if a new  $\overline{\text{RAS}}$  cycle occurs (as in hidden refresh). Each of the KM424C257 operating cycles is listed below after the corresponding output state produced by the cycle.

**Valid Output Data:** Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write, Read Color Register.

### Refresh

The data in the KM424C257 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the 512 rows every 8 ms. Any operation cycle performed in the RAM port refreshes the 2048 bits selected by the row addresses or an on-chip refresh address counter. Either a burst refresh or distributed refresh may be used. There are

several ways to accomplish this.

**$\overline{\text{RAS}}$ -Only Refresh:** This is the most common method for performing refresh. It is performed by strobing in a row address with  $\overline{\text{RAS}}$  while  $\overline{\text{CAS}}$  remains high. This cycle must be repeated for each of the 512 row address, ( $A_0$ - $A_8$ ).

**$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Refresh:** The KM424C257 has  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  on-chip refresh capability that eliminates the need for external refresh addresses. If  $\overline{\text{CAS}}$  is held low for the specified set up time ( $t_{CSA}$ ) before  $\overline{\text{RAS}}$  goes low the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle.

**Hidden Refresh:** A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the  $\overline{\text{CAS}}$  active time and cycling  $\overline{\text{RAS}}$ . The KM424C257 hidden refresh cycle is actually a  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

**Other Refresh Methods:** It is also possible to refresh the KM424C257 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general  $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh is the preferred method.

### Transfer Operation

1. Normal Write/Read Transfer (SAM→RAM/RAM→SAM.).
2. Pseudo Write Transfer (Switches serial port from serial Read to serial Write. No actual data transfer takes place between the RAM and the SAM.).
3. Real Time Read Transfer (On the fly Read Transfer operation).
4. Split Write/Read Transfer (Divides the SAM into a high and a low half. Only one half is transferred from/to the SAM while the other half is write to/read from the SDQ pins.).

### Read-Transfer Cycle

A read-transfer consists of loading a selected row of data from the RAM array into the SAM register. A read-transfer is accomplished by holding  $\overline{\text{CAS}}$  high,  $\overline{\text{DT}}/\overline{\text{OE}}$  low and  $\overline{\text{WB}}/\overline{\text{WE}}$  high at the falling edge of  $\overline{\text{RAS}}$ . The row address

**KM424C257****CMOS VIDEO RAM****DEVICE OPERATION** (Continued)

selected at the falling edge of  $\overline{RAS}$  determines the RAM row to be transferred into the SAM.

The actual data transfer completed at the rising edge of

data transfer. A pseudo write transfer is accomplished by holding  $\overline{CAS}$  high,  $\overline{DT}/\overline{OE}$  low,  $\overline{WB}/\overline{WE}$  low and  $\overline{SE}$  high at the falling edge of  $\overline{RAS}$ . The pseudo write transfer cycle must be performed after a read transfer cycle if

**Table 2. Truth table for Transfer operation**

RAS Falling Edge					Function	Transfer Direction	Transfer Data Bits	Sam port Mode
CAS	DT/OE	WB/WE	SE	DSF				
H	L	H	*	L	Read Transfer	RAM→SAM	512×4	Input→Output
H	L	L	L	L	Masked Write Transfer	SAM→RAM	512×4	Output→Input
H	L	L	H	L	Pseudo Write Transfer	—	—	Output→Input
H	L	H	*	H	Split Read Transfer	RAM→SAM	256×4	Not Changed
H	L	L	*	H	Split Write Transfer	SAM→RAM	256×4	Not Changed

\*: Don't Care

$\overline{DT}/\overline{OE}$ . When the transfer is completed, the SDQ lines are set into the output mode. In a read/real-time read-transfer cycle, the transfer of a new row of data is completed at the rising edge of  $\overline{DT}/\overline{OE}$  and becomes valid on the SDQ lines after the specified access time  $t_{SCA}$  from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of  $\overline{CAS}$ .

**Write Transfer Cycle**

A write transfer cycle consists of loading the content of the SAM data register into a selected row of RAM array. A write transfer is accomplished by  $\overline{CAS}$  high,  $\overline{DT}/\overline{OE}$  low,  $\overline{WB}/\overline{WE}$  low and  $\overline{SE}$  low at the falling edge of  $\overline{RAS}$ . The row address selected at the falling edge of  $\overline{RAS}$  determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of  $\overline{CAS}$  determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SDQ lines are in the input mode so that serial data synchronized with SC can be loaded. When two consecutive write transfer operations are performed, there is a delay in availability between the last bit of the previous row and the first bit of the new row. Consequently the SC clock must be held at a constant  $V_{IL}$  or  $V_{IH}$  after the SC precharge time  $t_{SCP}$  has been satisfied, a rising edge of the SC clock until after a specified delay  $t_{SRD}$  from the rising edge of  $\overline{RAS}$ .

**Pseudo Write Transfer Cycle**

The pseudo write transfer cycle switches SDQ lines from serial read mode to serial write mode. It doesn't perform

the subsequent operation is a write transfer cycle. There is a timing delay associated with the switching of the SDQ lines from serial output mode to serial input mode. During this period, the SC clock must be held at a constant  $V_{IL}$  or  $V_{IH}$  after the  $t_{SC}$  precharge time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay  $t_{SRD}$  from the rising edge of  $\overline{RAS}$ .

**Special Function Input (DSF)**

In read transfer mode, holding DSF high on the falling edge of  $\overline{RAS}$  selects the split register mode read transfer operation. This mode divides the serial data register into a high order half and a low order half; one active, and one inactive. When the cycle is initiated, a transfer occurs between the memory array and either the high half or the low half register, depending on the state of most significant column address bit ( $A_8$ ) that is strobed in on the falling edge of  $\overline{CAS}$ . If  $A_8$  is high, the transfer is to the high half of the register. If  $A_8$  is low, the transfer is to the low half of the register. Use of the split register mode read transfer feature allows on-the-fly read transfer operation without synchronizing  $\overline{DT}/\overline{OE}$  to the serial clock. The transfer can be to either the active half or the inactive half register. If the transfer is to the active register, with an uninterrupted serial data stream, then the timings  $t_{RSL}$  and  $t_{RSD}$  must be met.

In write transfer mode, holding DSF high on the falling edge of  $\overline{RAS}$  permits use of a Split Register mode of transfer write. This mode allows  $\overline{SE}$  to be high on the falling edge of  $\overline{RAS}$  without performing a pseudo write transfer, with the serial port disabled during the entire transfer write cycle.

**KM424C257****CMOS VIDEO RAM****DEVICE OPERATION** (Continued)**Split Register Active Status Output (QSF)**

QSF indicates which half of the serial register in the SAM is being accessed. If QSF is low, then the serial address pointer is accessing the low (least significant) 256 bits of the SAM. If QSF is high, then the pointer is accessing the higher (most significant) 256 bits of the SAM.

**Serial Clock (SC)**

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SDQ pins after the maximum specified serial access time  $t_{SCA}$  from the rising edge of SC. The serial clock SC also increments the 9 bit serial pointer which is used to select the SAM address. The pointer address is incremented in a wrap around mode to select sequential locations after the starting location which is determined by the column address in the read transfer cycle.

**Serial Input/Output (SDQ<sub>0</sub>-SDQ<sub>3</sub>)**

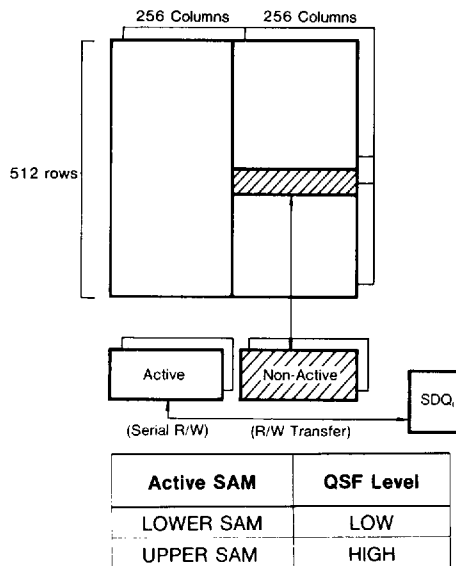
Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a pseudo write is performed, the SAM port operation is switched from output mode to input mode. During subsequent write transfer cycle, the SAM port remains in the input mode.

**Tap Address Limitation**

The Tap Address of non-split transfer cycle preceding split transfer cycle should be between 0 and 253 or between 256 and 509.

**Power-up**

An initial pause of 200  $\mu$ sec is required after power-up followed by 8 initialization cycles before proper device operation is assured.

**Table 3. SPLIT REGISTER MODE**

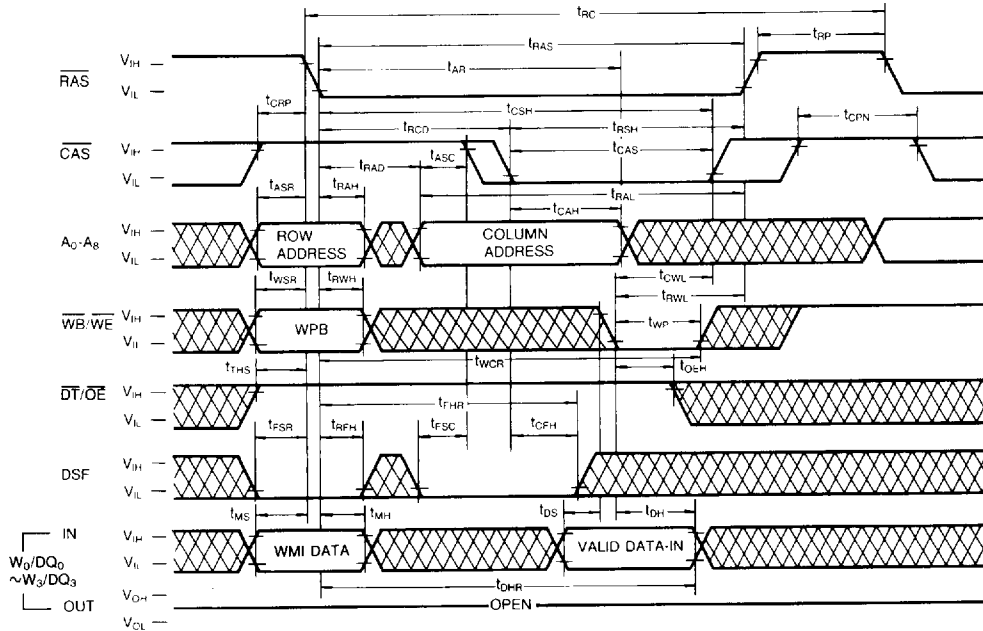


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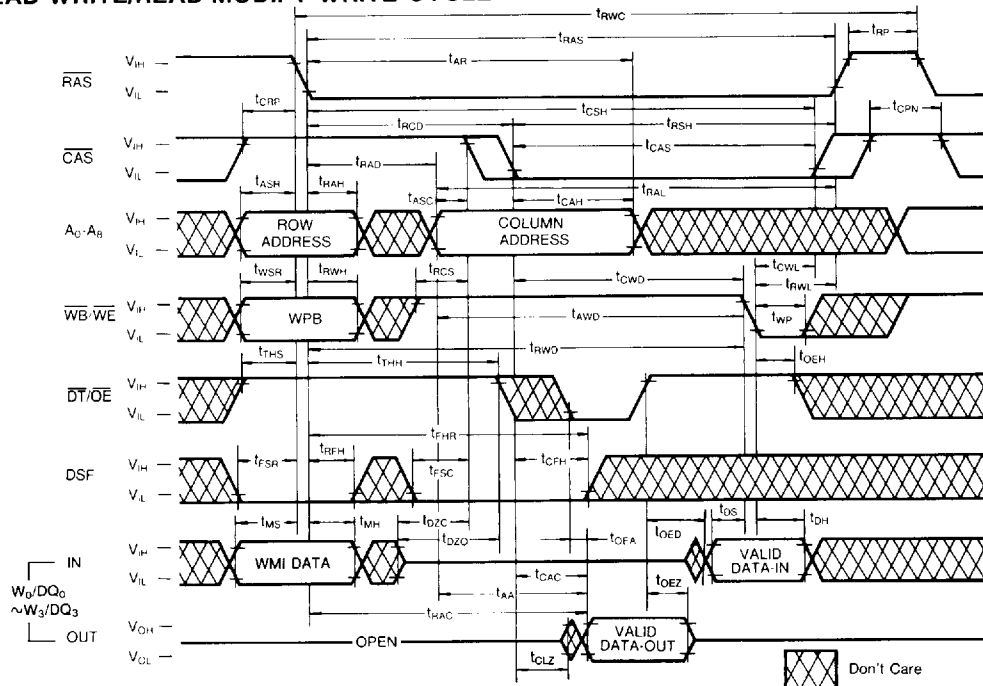
**CMOS VIDEO RAM**

**TIMING DIAGRAMS** (Continued)

**WRITE CYCLE ( $\overline{OE}$  CONTROLLED WRITE)**



**READ-WRITE/READ-MODIFY-WRITE CYCLE**



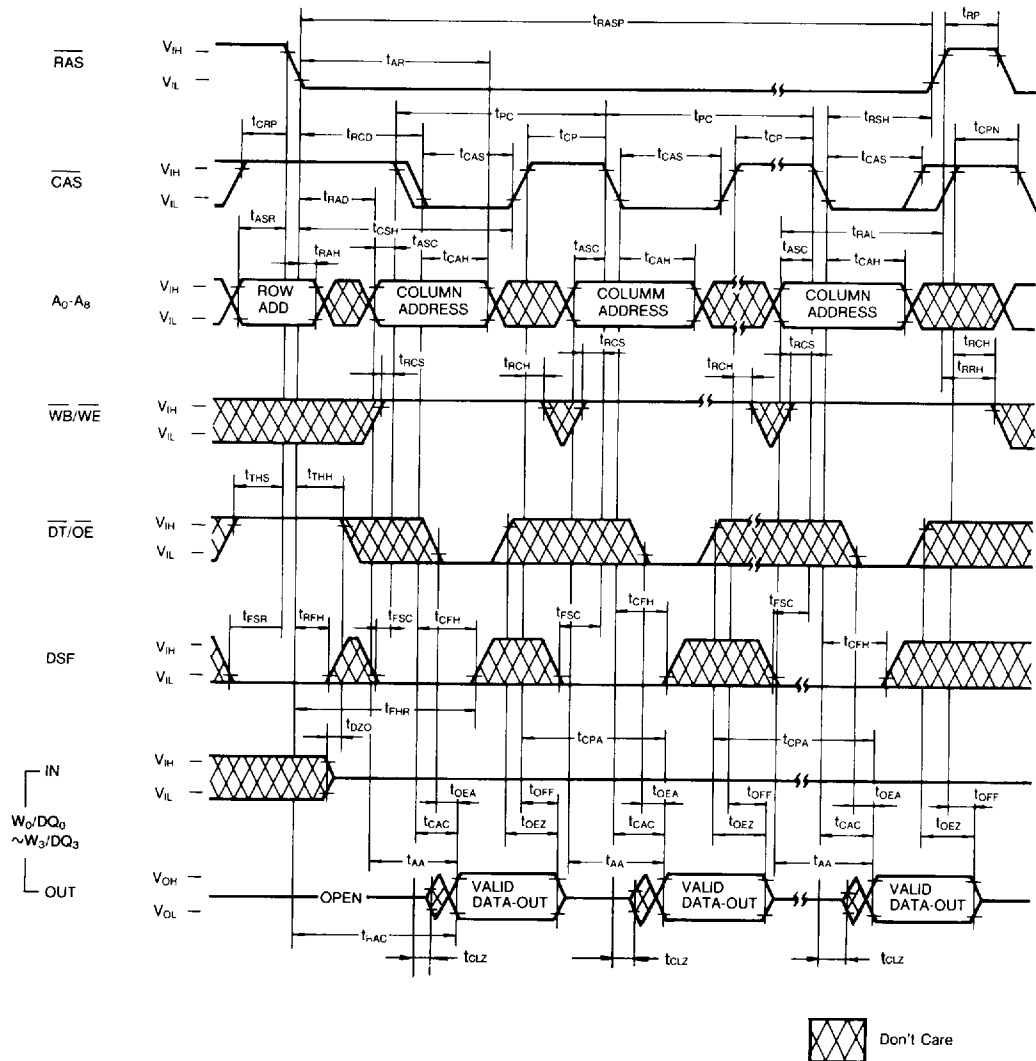
2

## KM424C257

## CMOS VIDEO RAM

## TIMING DIAGRAMS (Continued)

## PAGE MODE READ CYCLE



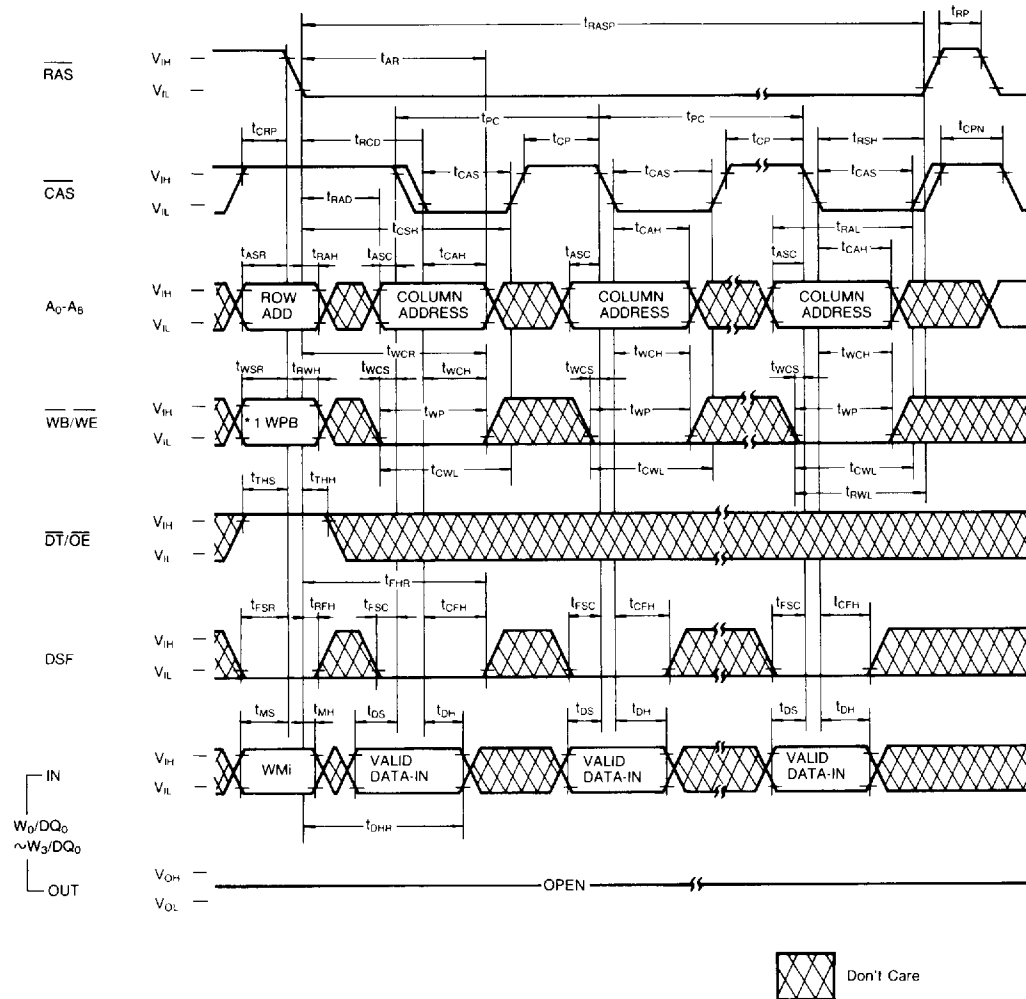


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**CMOS VIDEO RAM**

**TIMING DIAGRAMS** (Continued)

**PAGE MODE WRITE CYCLE (EARLY WRITE)**



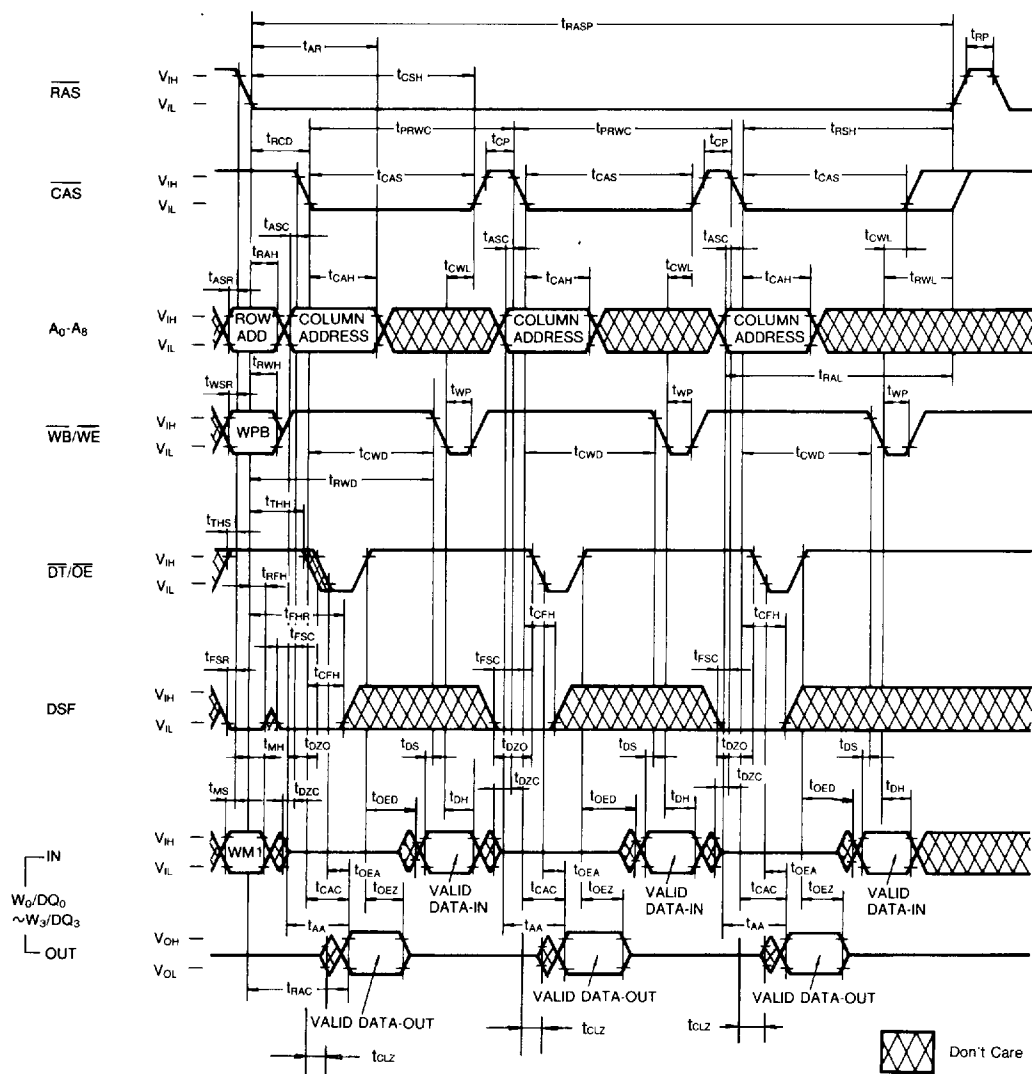
2

**KM424C257**

**CMOS VIDEO RAM**

**TIMING DIAGRAMS** (Continued)

**PAGE MODE READ-MODIFY-WRITE CYCLE**

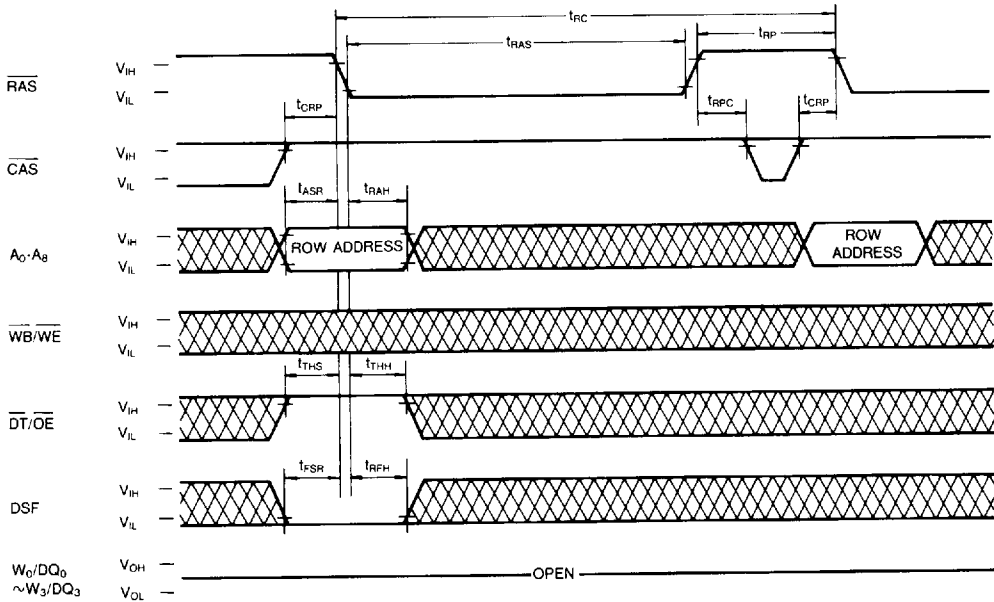


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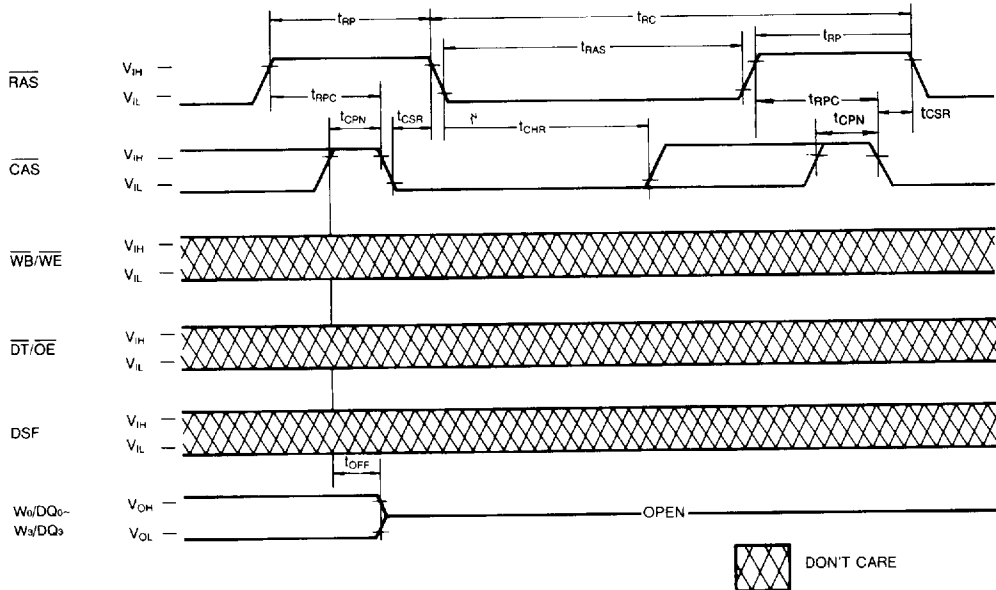
**CMOS VIDEO RAM**

**TIMING DIAGRAMS** (Continued)

**RAS ONLY REFRESH CYCLE**



**CAS BEFORE RAS REFRESH**



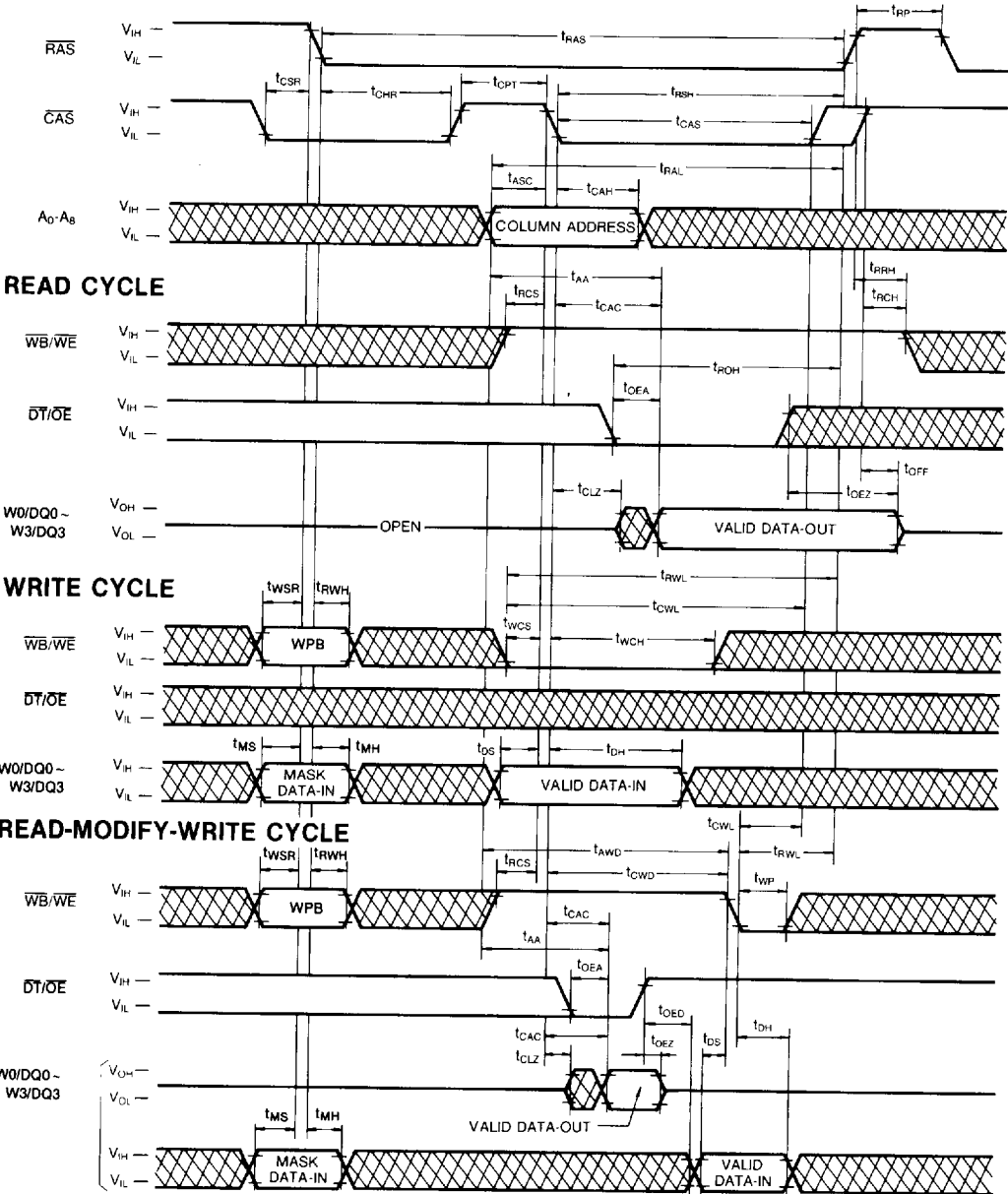
2

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**CMOS VIDEO RAM**

**TIMING DIAGRAMS (Continued)**

**CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE**



DSF = DON'T CARE

 DON'T CARE

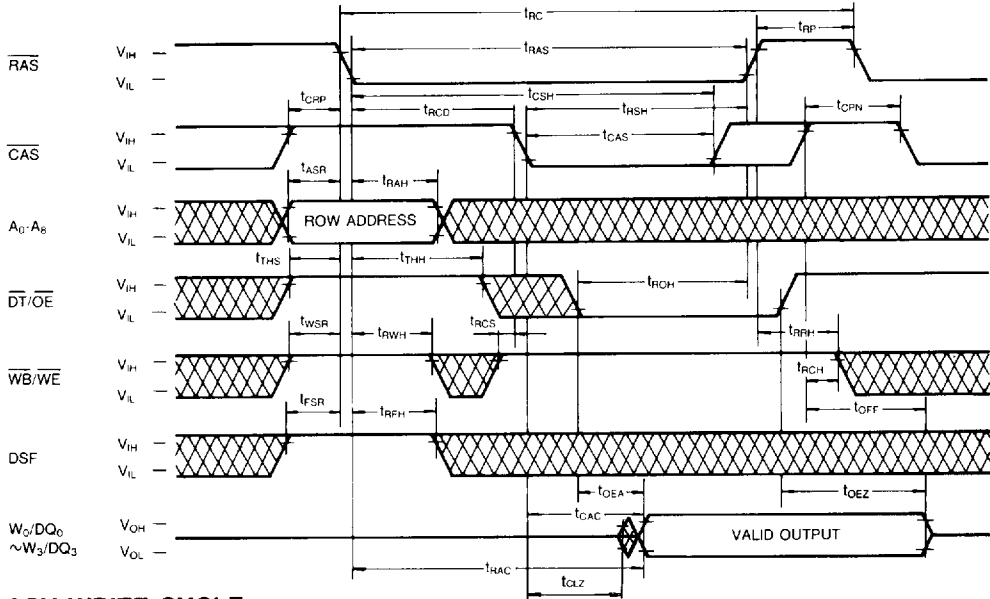


# KM424C257

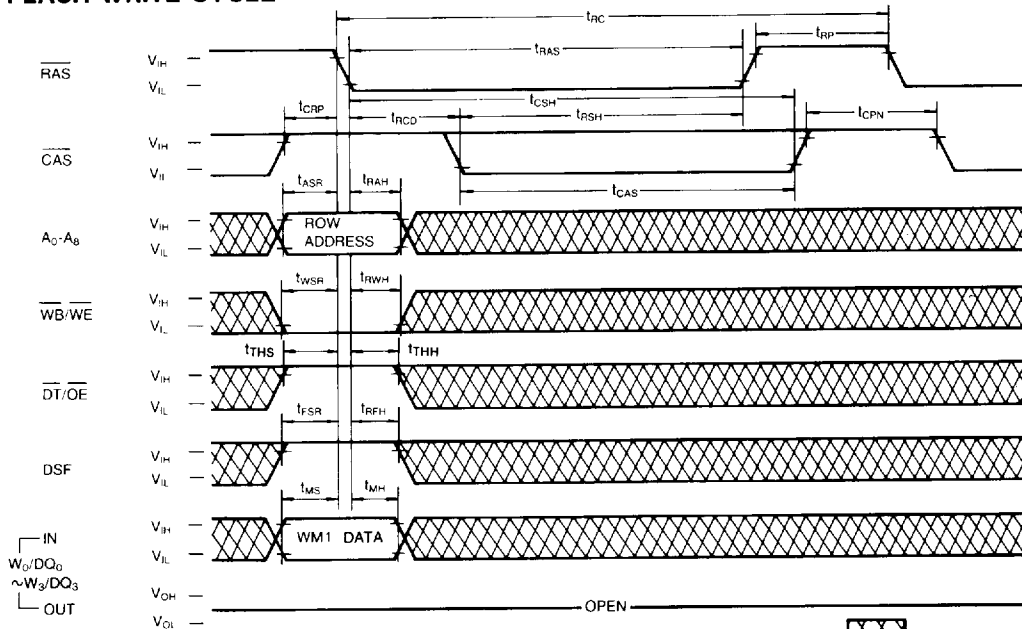
# CMOS VIDEO RAM

## TIMING DIAGRAMS (Continued)

### READ COLOR REGISTER CYCLE



### FLASH WRITE CYCLE



WM1 DATA	CYCLE
0	Flash write Disable
1	Flash write Enable

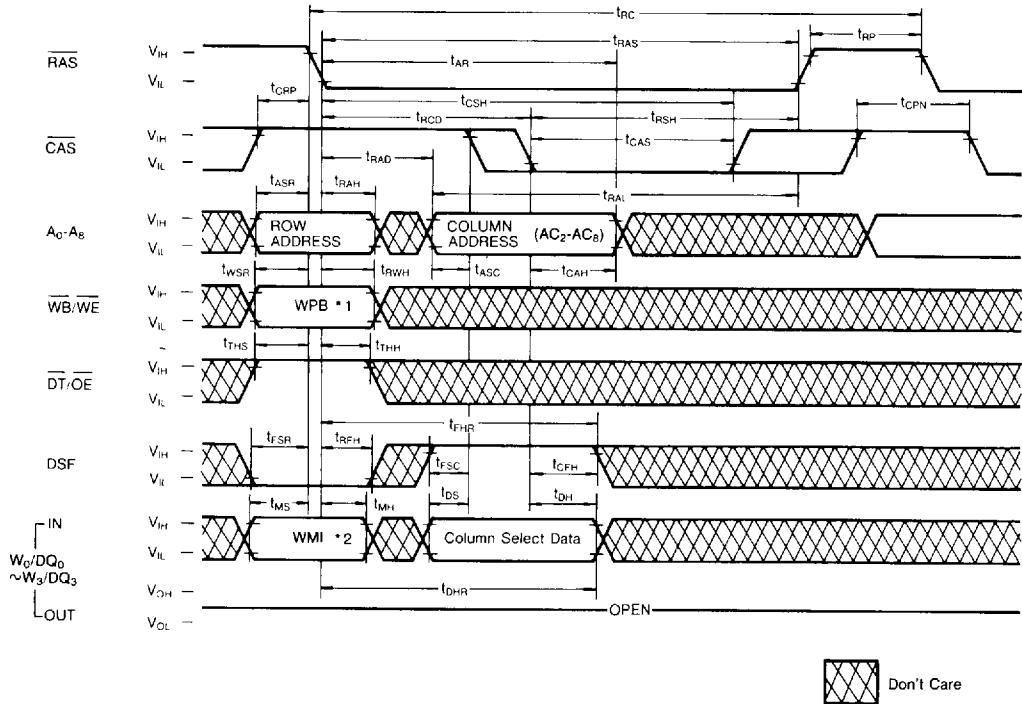
 Don't Care

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**CMOS VIDEO RAM**

**TIMING DIAGRAMS** (Continued)

**BLOCK WRITE CYCLE**



2

*1 WB/WE	*2 W0/DQ0-W3/DQ3	CYCLE
0	WM1 Data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

WM1 Data: 0: Write Disable  
1: Write Enable

COLUMN SELECT DATA  
 W0/DQ0 — Column 0 (A<sub>1C</sub>=0, A<sub>0C</sub>=0)  
 W1/DQ1 — Column 1 (A<sub>1C</sub>=0, A<sub>0C</sub>=1)  
 W2/DQ2 — Column 2 (A<sub>1C</sub>=1, A<sub>0C</sub>=0)  
 W3/DQ3 — Column 3 (A<sub>1C</sub>=1, A<sub>0C</sub>=1)

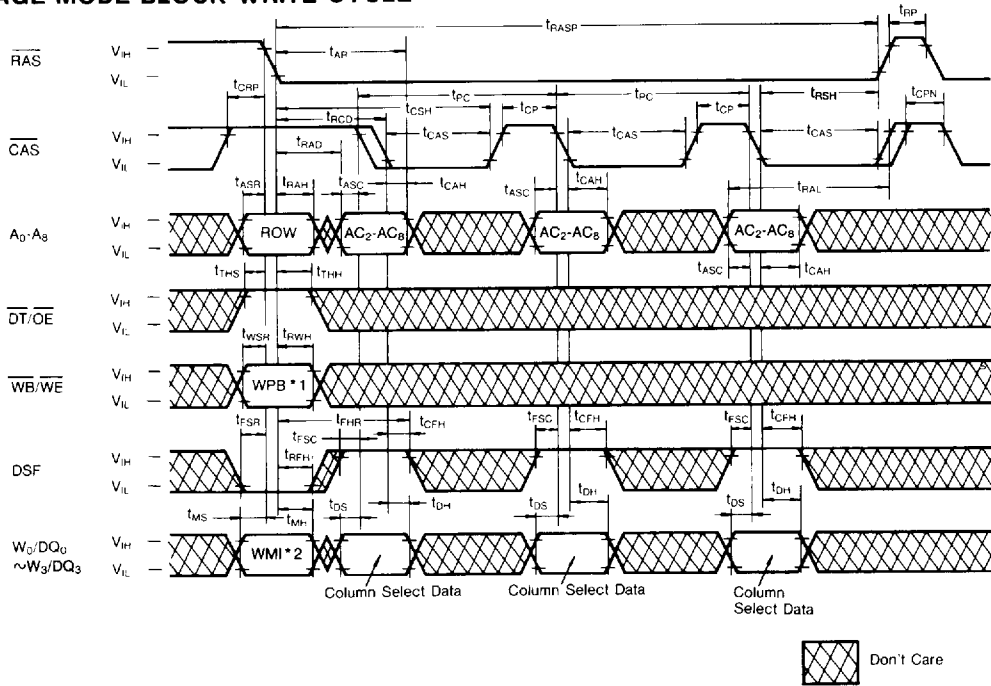
Wn/DQn  
 = 0: Disable  
 = 1: Enable

# KM424C257

# CMOS VIDEO RAM

## TIMING DIAGRAMS (Continued)

### PAGE MODE BLOCK WRITE CYCLE



*1 WB/WE	*2 W0/DQ0-W3/DQ3	CYCLE
0	WM1 Data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

WM1 Data: 0: Write Disable  
1: Write Enable

#### COLUMN SELECT DATA

W0/DQ0 — Column 0 (A<sub>1C</sub>=0, A<sub>0C</sub>=0)  
 W1/DQ1 — Column 1 (A<sub>1C</sub>=0, A<sub>0C</sub>=1)  
 W2/DQ2 — Column 2 (A<sub>1C</sub>=1, A<sub>0C</sub>=0)  
 W3/DQ3 — Column 3 (A<sub>1C</sub>=1, A<sub>0C</sub>=1)

Wn/DQn  
 = 0: Disable  
 = 1: Enable



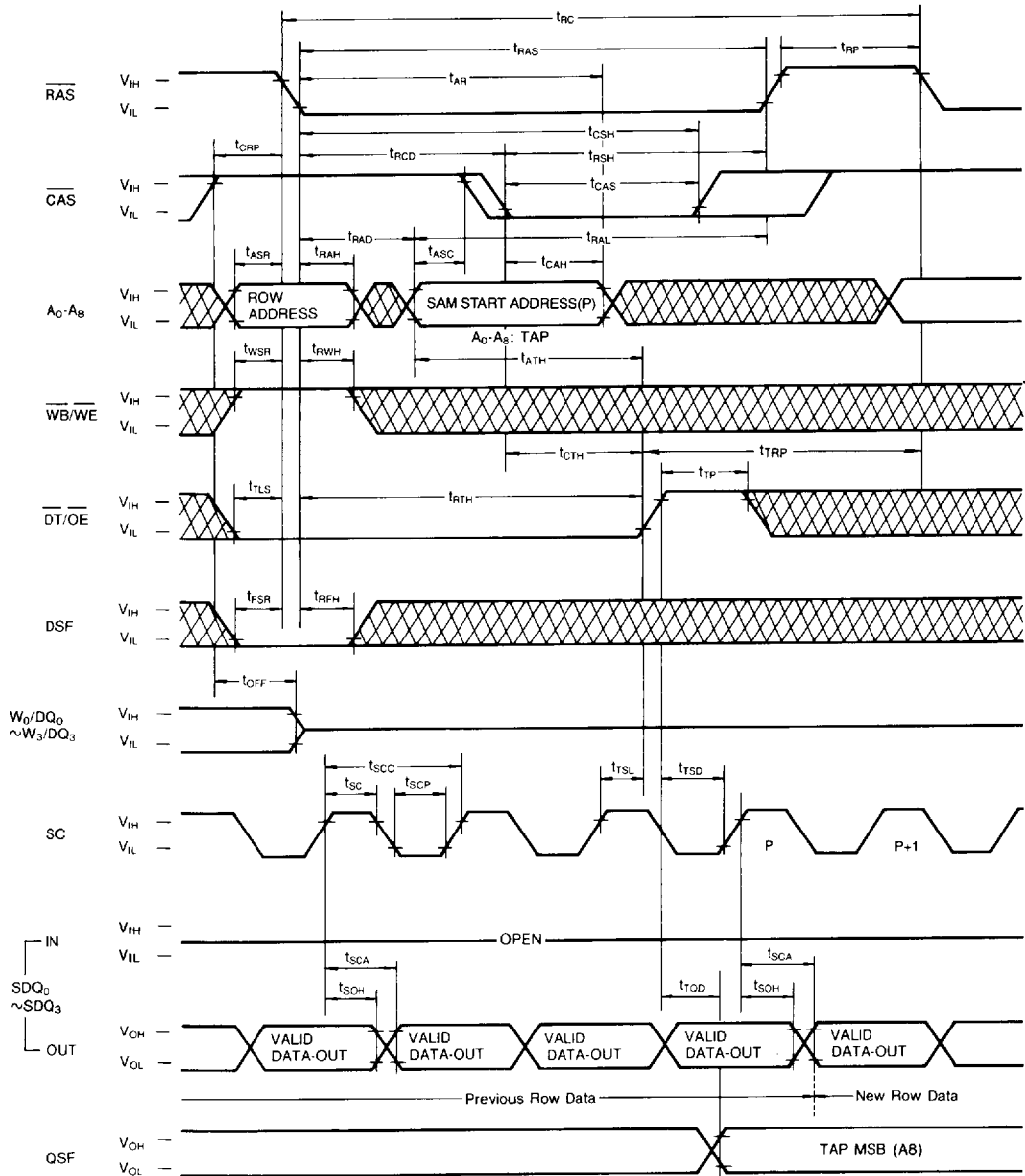


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**CMOS VIDEO RAM**

**TIMING DIAGRAMS** (Continued)

**REAL TIME READ TRANSFER CYCLE**



Note:  $\overline{SE} = V_{IL}$

 Don't Care

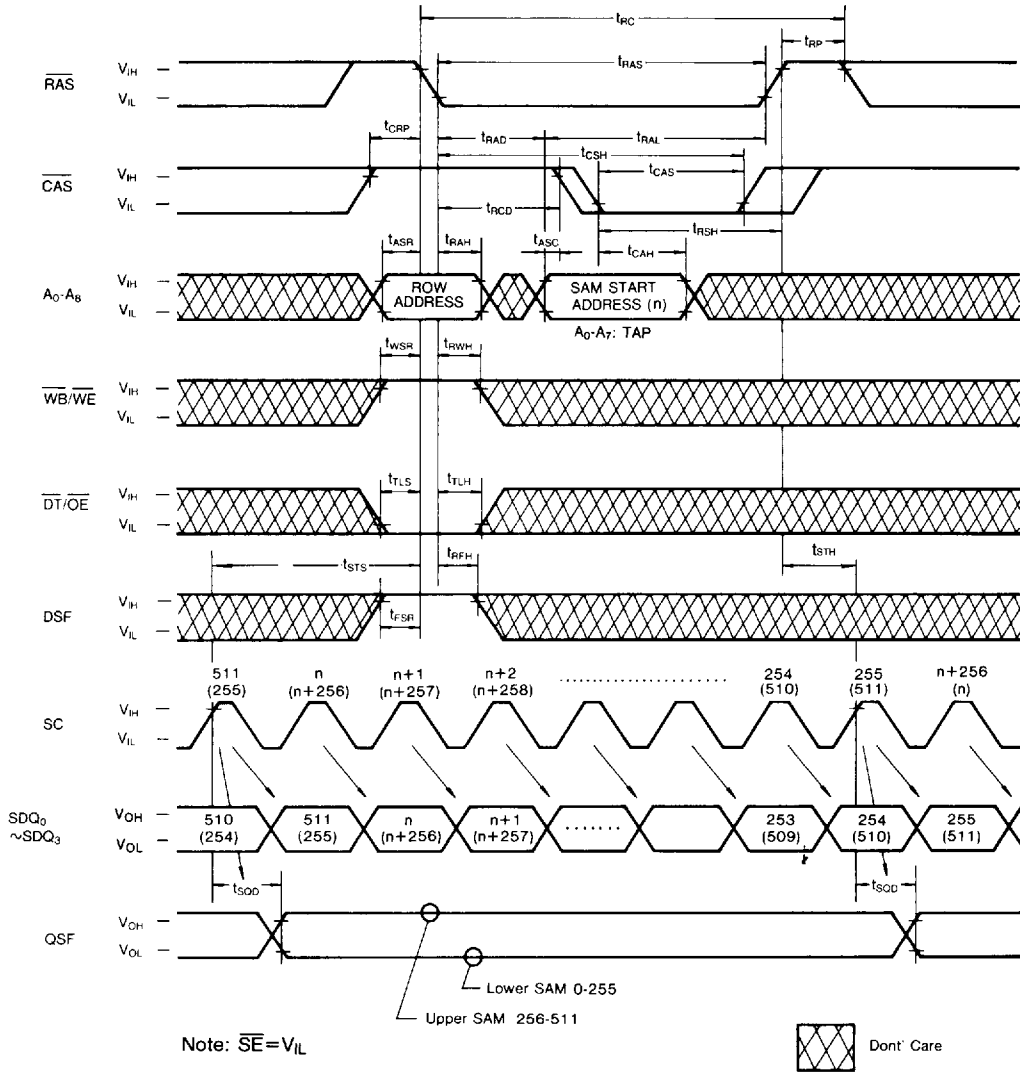
**KM424C257**

**CMOS VIDEO RAM**

**TIMING DIAGRAMS** (Continued)

**SPLIT READ TRANSFER CYCLE**

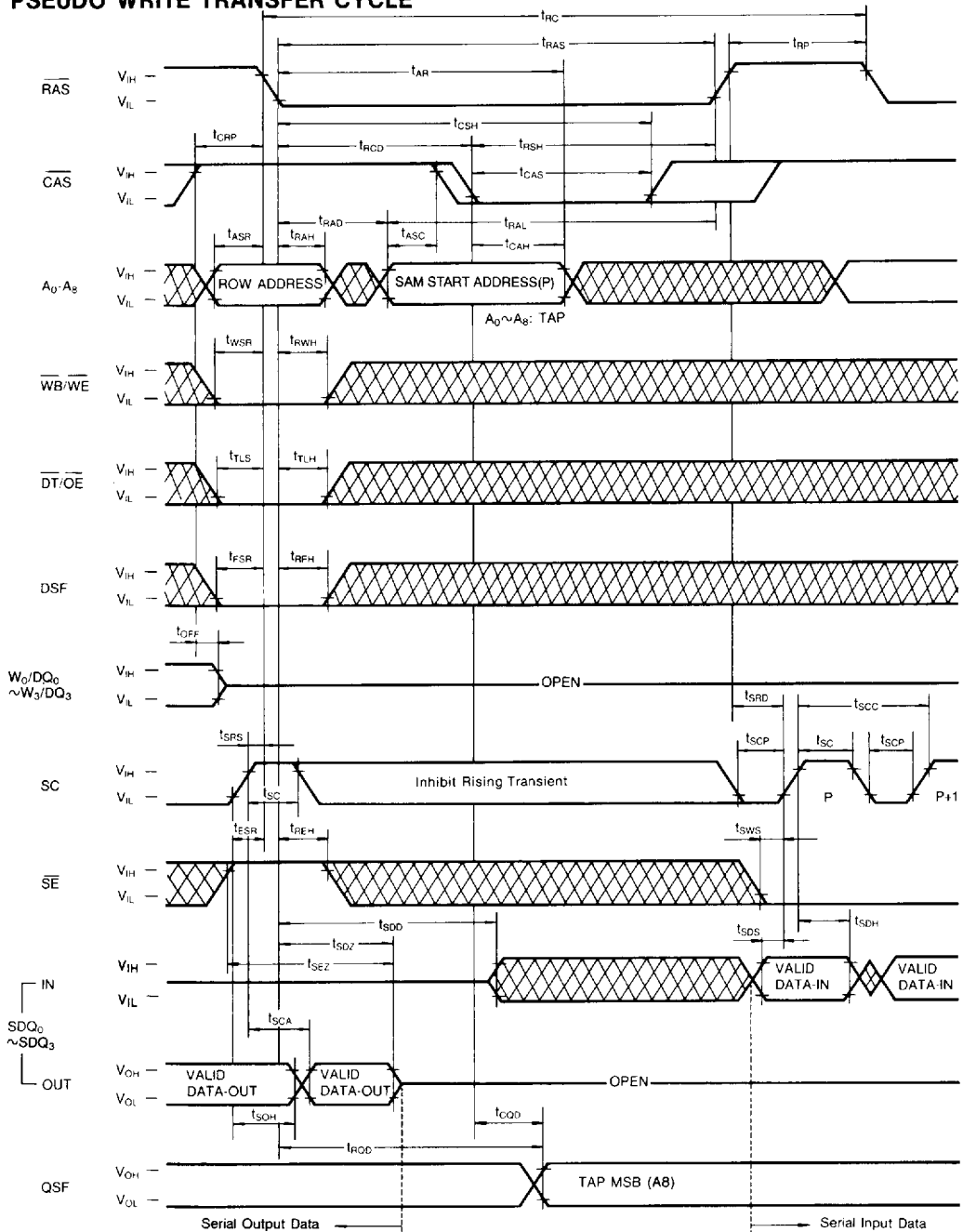
2



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**CMOS VIDEO RAM**

**TIMING DIAGRAMS (Continued)**  
**PSEUDO WRITE TRANSFER CYCLE**

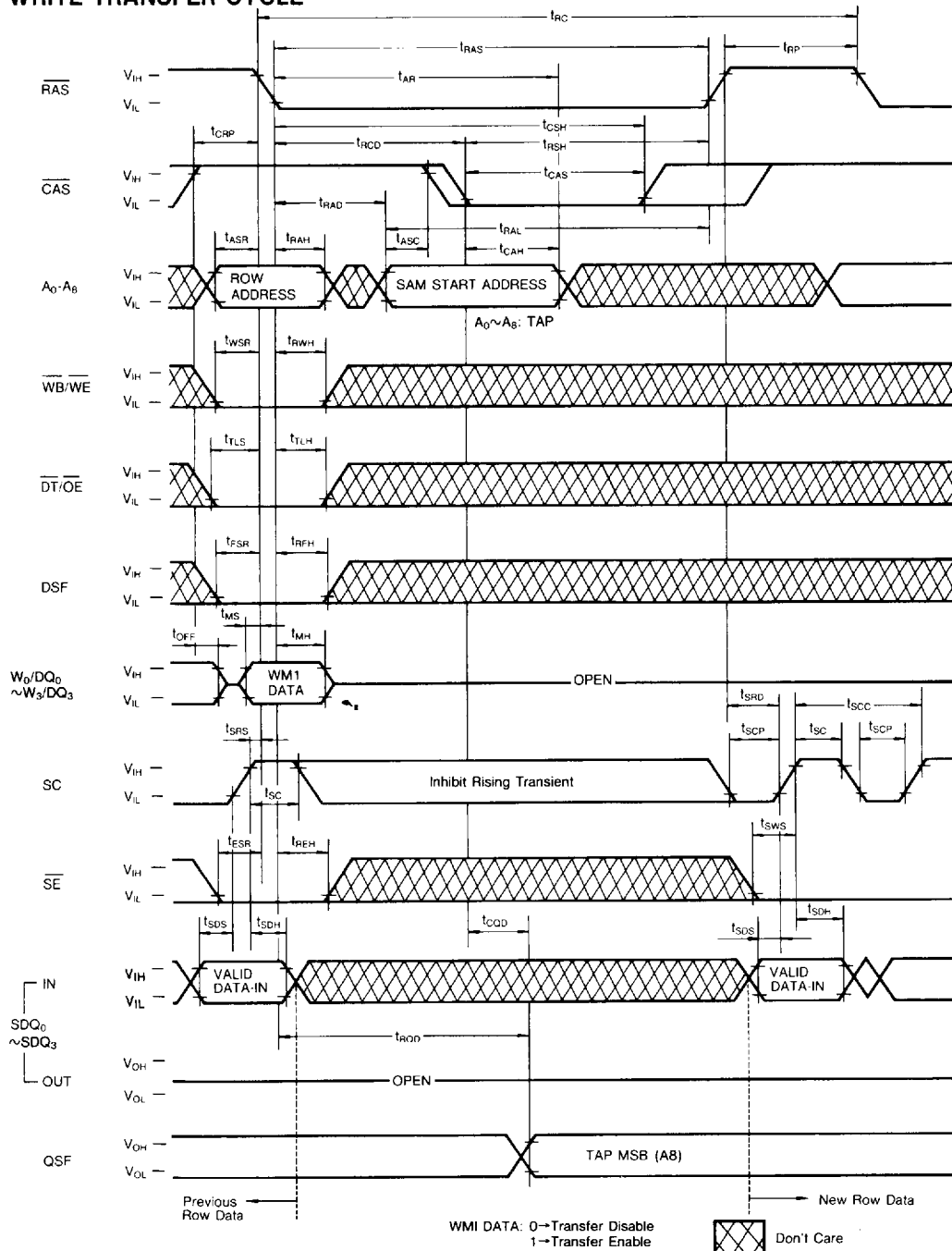


# KM424C257

# CMOS VIDEO RAM

## TIMING DIAGRAMS (Continued)

### WRITE TRANSFER CYCLE



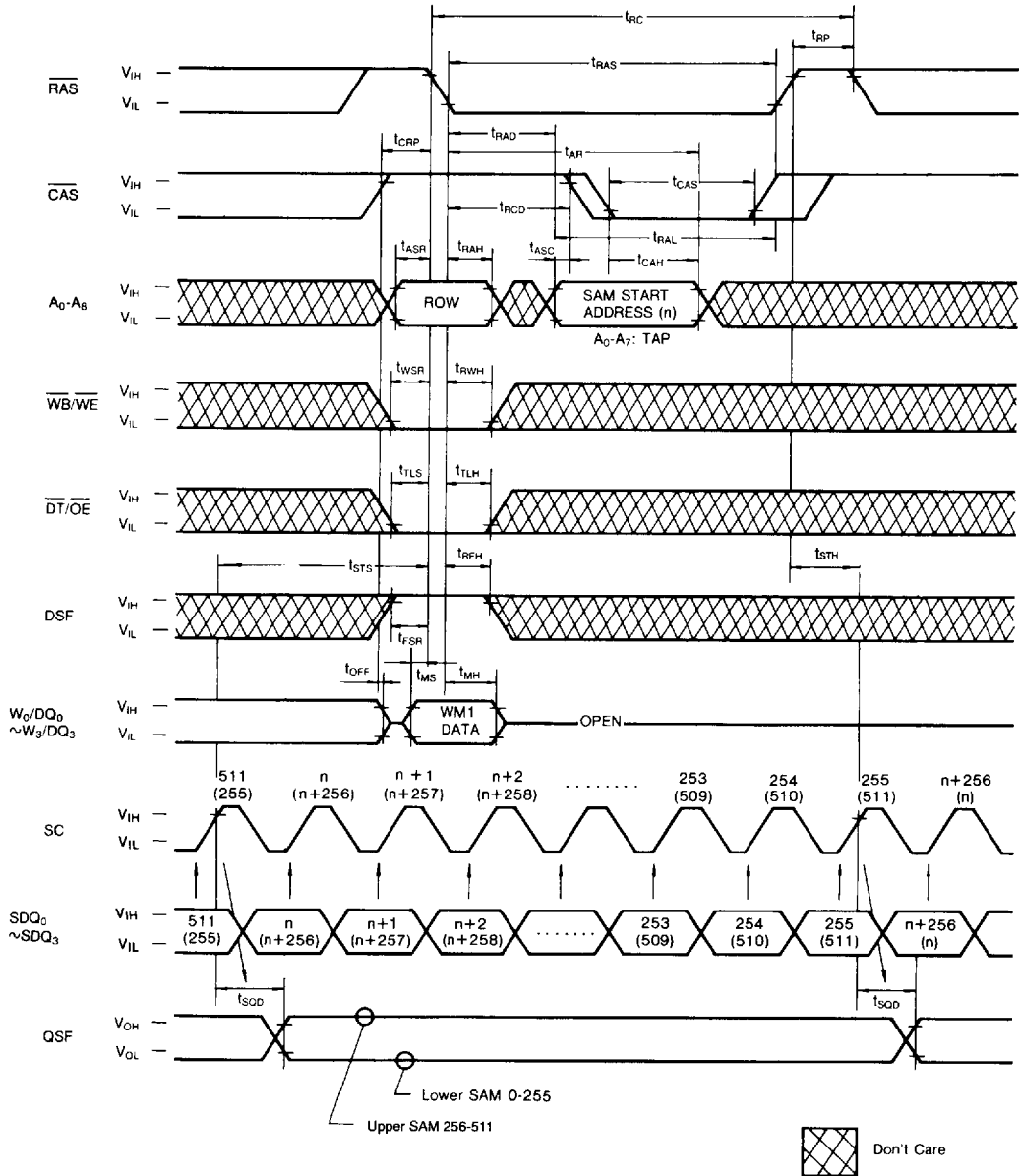
2

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**CMOS VIDEO RAM**

**TIMING DIAGRAMS** (Continued)

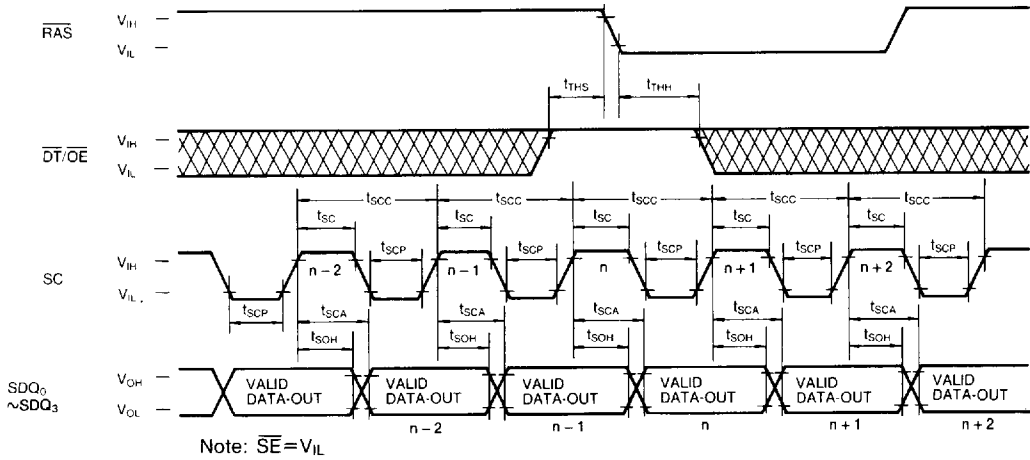
**SPLIT WRITE TRANSFER CYCLE**



**KM424C257**

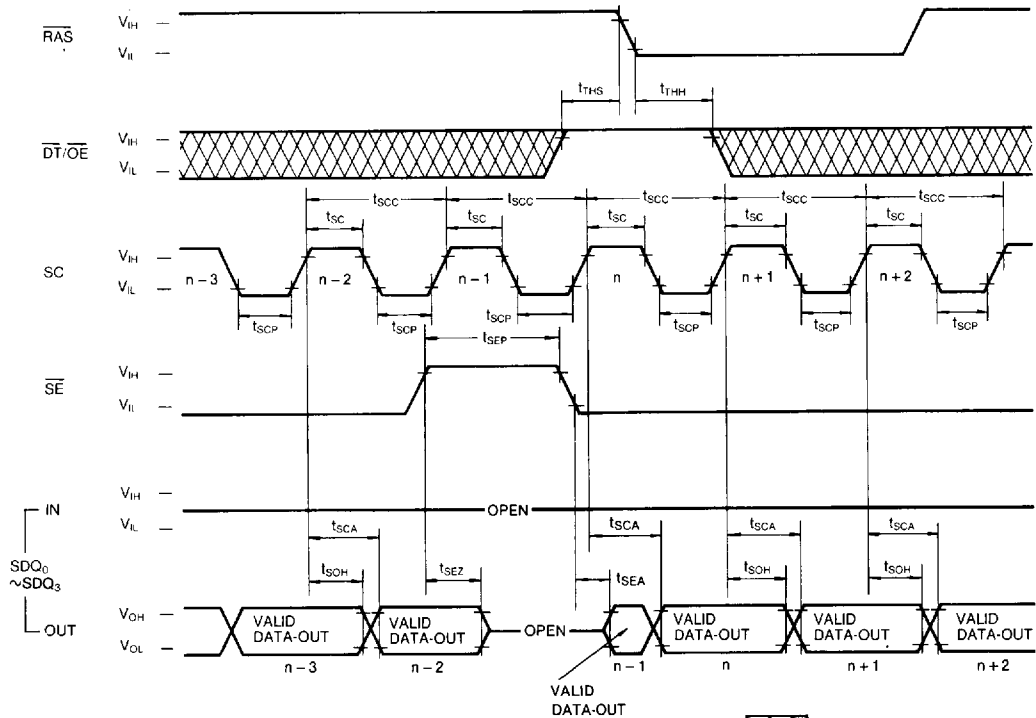
**CMOS VIDEO RAM**

**SERIAL READ CYCLE ( $\overline{SE} = V_{IL}$ )**



2

**SERIAL READ CYCLE ( $\overline{SE}$  Controlled Outputs)**



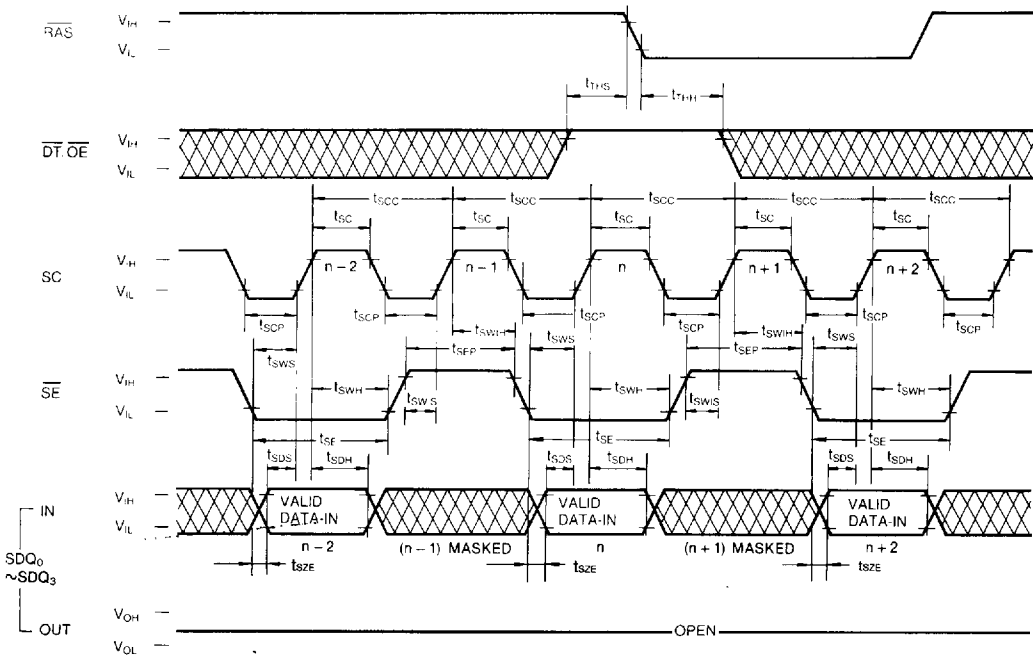
 Don't Care

# KM424C257

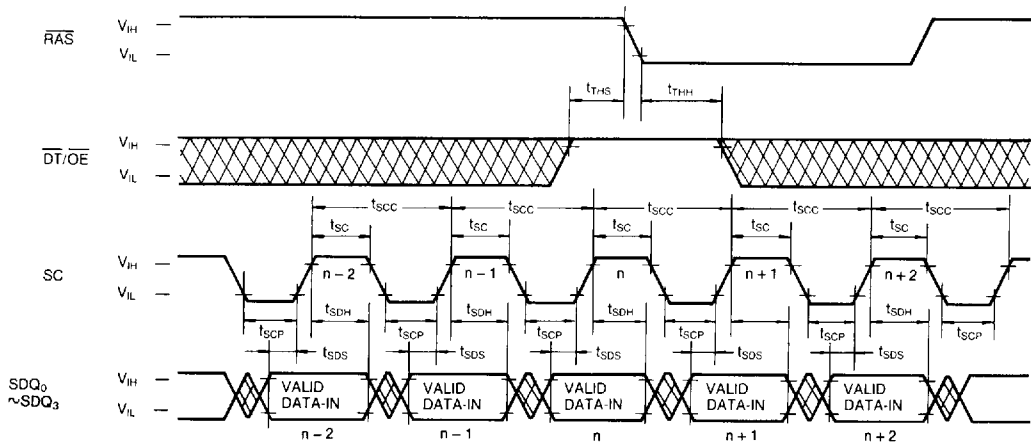
# CMOS VIDEO RAM

## TIMING DIAGRAMS (Continued)

### SERIAL WRITE CYCLE ( $\overline{SE}$ Controlled Inputs)



### SERIAL WRITE CYCLE ( $\overline{SE} = V_{IL}$ )



Note:  $\overline{SE} = V_{IL}$





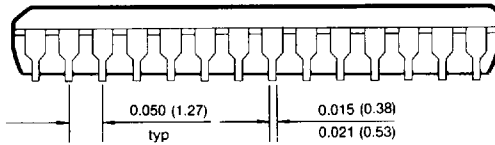
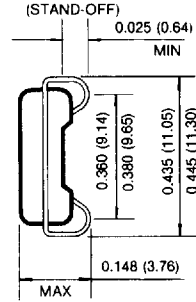
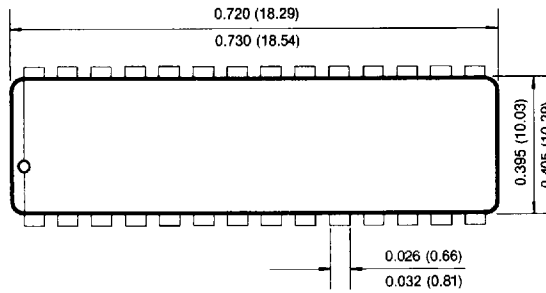
# KM424C257

# CMOS VIDEO RAM

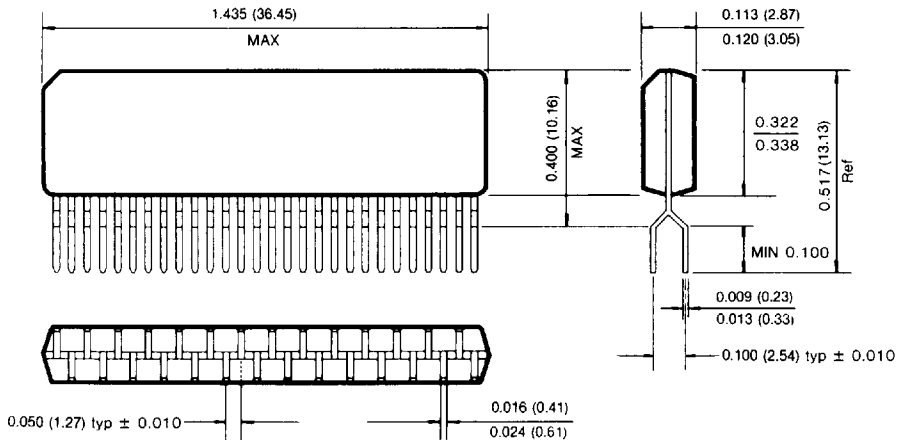
## PACKAGE DIMENSIONS

### 28-PIN PLASTIC SOJ

Units Inches (millimeters)



### 28-PIN PLASTIC ZIP



2