# SK hynix e-NAND™ Product Family

# eMMC4.5 Compatible

## Revision History

| Revision No. | History | Draft Date | Remark |
|---|---|---|---|
| 0.1 | Preliminary | Fab. 04, 2014 | |
| 0.2 | Updated power consumption<br>-. Added peak current value [p8_Power_Active power consumption]<br>-. Updated average current value [p8_Power active / Standby / Sleep current] | Mar. 19, 2014 | |
| 0.3 | Updated Register value<br>-. Revised PNM value [p31_CID field] | July. 03, 2014 | |

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# 1. Introduction

## 1.1 General description

SK hynix e-NAND consists of NAND flash and MMC controller.
e-NAND has the built-in intelligent controller which manages interface protocols, wear leveling, bad block management, garbage collection, and ECC. e-NAND protects the data contents from the host sudden power off failure.
e-NAND is compatible with JEDEC standard eMMC4.5 specification.

## 1.2 Product list

| Density | Part Number | NAND Flash Type | PKG size (mm) | Package Type |
|---|---|---|---|---|
| 4GB | H26M31001HPR | 32Gb x 1 | 11.5x13x0.8 | 153FBGA |

## 1.3 Key features

- **eMMC4.5 compatible**
  (Backward compatible to eMMC4.41)

- **Bus mode**
  - Data bus width : 1 bit(default), 4 bits, 8 bits
  - Data transfer rate: up to 200MB/s (HS200)
  - MMC I/F Clock frequency : 0~200MHz
  - MMC I/F Boot frequency : 0~52MHz

- **Operating voltage range**
  - $V_{cc}$ (NAND) : 2.7 - 3.6V
  - $V_{ccq}$ (Controller) : 1.7 - 1.95V / 2.7 - 3.6V

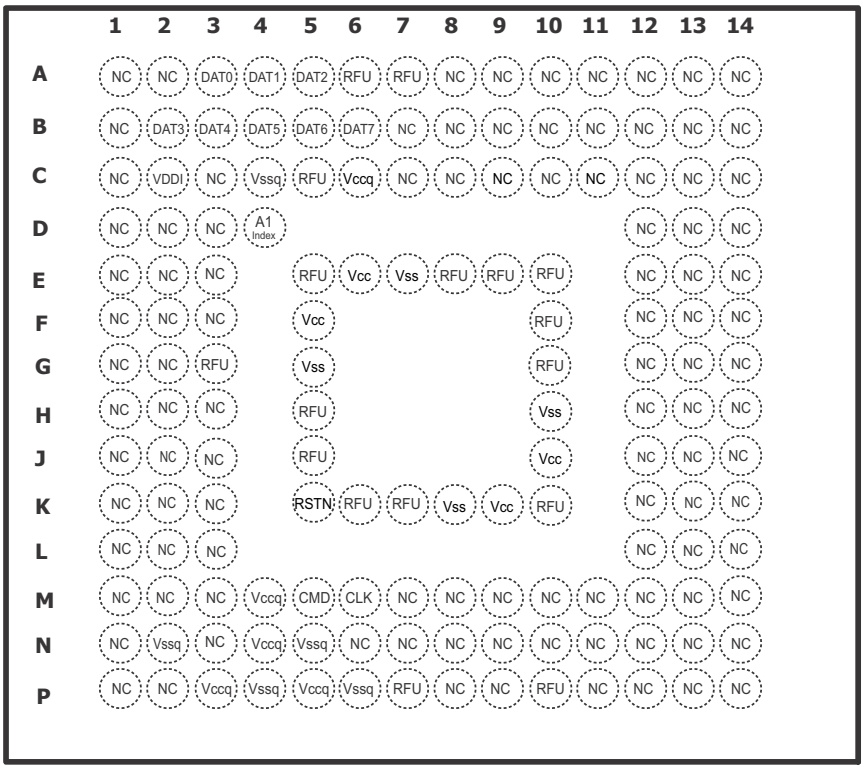
- **Temperature**
  - Operation (-25℃ ~ +85℃)
  - Storage without operation (-40℃ ~ +85℃)

- **Others**
  - This product is compliance with the RoHS directive

- **Supported features**
  - HS200
  - HPI, BKOPS
  - Packed CMD, Cache, Data tag, Context ID
  - Partitioning, RPMB
  - Discard, Trim, Erase, Sanitize, Secure TRIM,
  - Write protect, Lock / Unlock
  - PON, Sleep / Awake
  - Reliable write
  - Boot feature, Boot partition
  - HW / SW Reset
  - Health(Smart) report

# 2. Package Configurations

## 2.1 Pin connection




**[Figure 1]FBGA153 Package connections (Top view through package)**

| Pin number | Name | Pin number | Name | Pin number | Name | Pin number | Name |
|---|---|---|---|---|---|---|---|
| **A3** | DAT0 | **C2** | VDDi | **J10** | $V_{cc}$ | **N4** | $V_{ccq}$ |
| **A4** | DAT1 | **C4** | $V_{ssq}$ | **K5** | RSTN | **N5** | $V_{ssq}$ |
| **A5** | DAT2 | **C6** | $V_{ccq}$ | **K8** | $V_{ss}$ | **P3** | $V_{ccq}$ |
| **B2** | DAT3 | **E6** | $V_{cc}$ | **K9** | $V_{cc}$ | **P4** | $V_{ssq}$ |
| **B3** | DAT4 | **E7** | $V_{ss}$ | **M4** | $V_{ccq}$ | **P5** | $V_{ccq}$ |
| **B4** | DAT5 | **F5** | $V_{cc}$ | **M5** | CMD | **P6** | $V_{ssq}$ |
| **B5** | DAT6 | **G5** | $V_{ss}$ | **M6** | CLK | | |
| **B6** | DAT7 | **H10** | $V_{ss}$ | **N2** | $V_{ssq}$ | | |

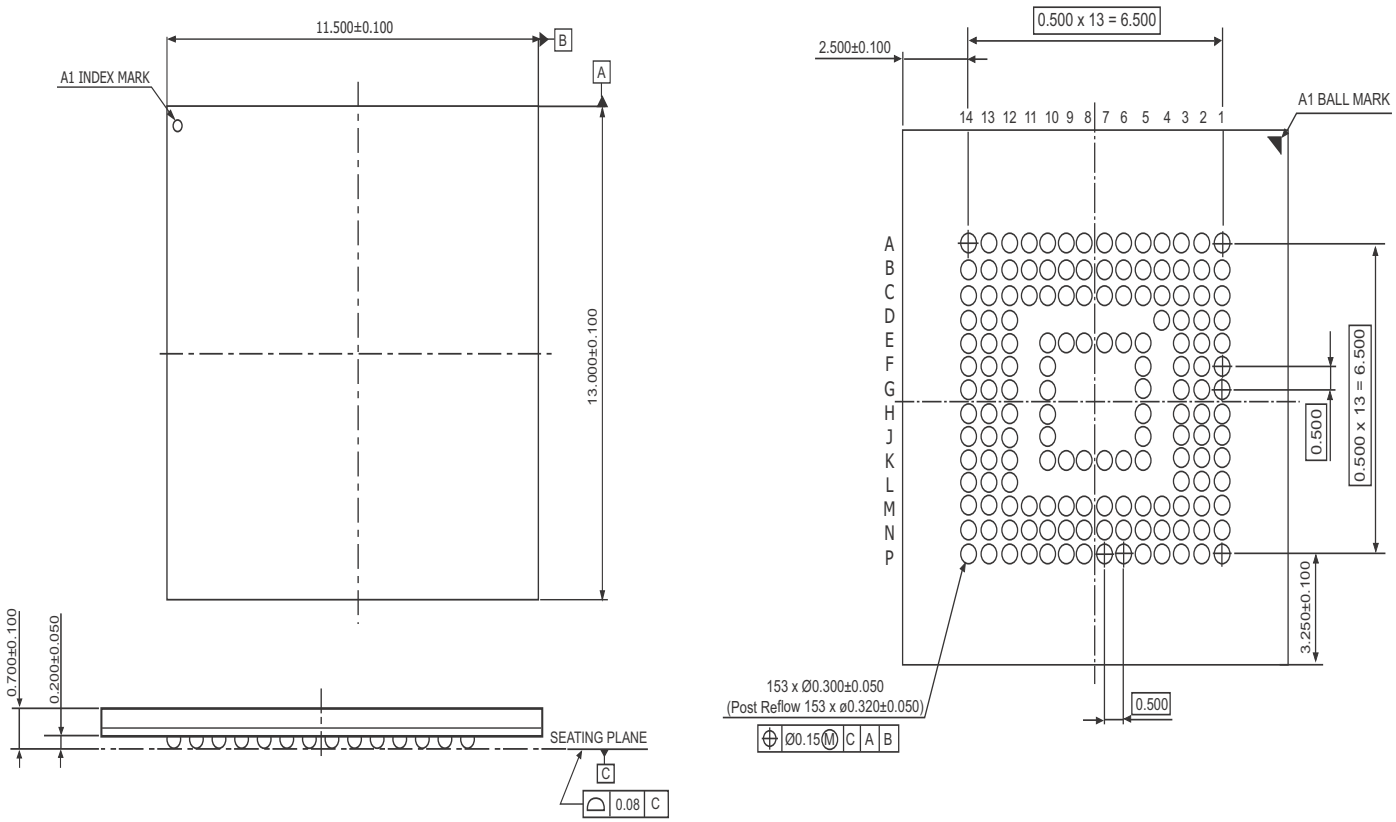
| Symbol | Type | Ball No. | Ball function |
|---|---|---|---|
| CLK | Input | M6 | Clock: Each cycle directs a 1-bit transfer on the command and DAT lines. |
| CMD | Input | M5 | Command:<br>A bidirectional channel used for device initialization and command transfers.<br>Command has two operating modes:<br>1) Open-drain for initialization.<br>2) Push-pull for fast command transfer. |
| DAT0 | I/O | A3 | Data I/O0: Bidirectional channel used for data transfer. |
| DAT1 | I/O | A4 | Data I/O1: Bidirectional channel used for data transfer. |
| DAT2 | I/O | A5 | Data I/O2: Bidirectional channel used for data transfer. |
| DAT3 | I/O | B2 | Data I/O3: Bidirectional channel used for data transfer. |
| DAT4 | I/O | B3 | Data I/O4: Bidirectional channel used for data transfer. |
| DAT5 | I/O | B4 | Data I/O5: Bidirectional channel used for data transfer. |
| DAT6 | I/O | B5 | Data I/O6: Bidirectional channel used for data transfer. |
| DAT7 | I/O | B6 | Data I/O7: Bidirectional channel used for data transfer. |
| RSTN | Input | K5 | Reset signal pin |
| $V_{cc}$ | Supply | E6, F5, J10, K9 | $V_{cc}$: Flash memory I/F and Flash memory power supply. |
| $V_{ccq}$ | Supply | C6, M4, N4, P3, P5 | $V_{ccq}$: Memory controller core and MMC interface I/O power supply. |
| Vss | Supply | E7, G5, H10, K8 | $V_{ss}$: Flash memory I/F and Flash memory ground connection. |
| Vssq | Supply | C4, N2, N5, P4, P6 | $V_{ssq}$: Memory controller core and MMC I/F ground connection |
| VDDi | | C2 | VDDi: Connect 0.1uF capacitor from VDDi to ground. |
| RFU | Reserved for future use | | |

**[Table 1]FBGA153 Ball description**

## 2.2 Package mechanical drawing

■ **11.5mm x13.0mm x0.8mm**

**Top view** **Bottom view**




**[Figure 2]11.5mm x 13.0mm x 0.8mm Package dimension**

# 3. e-NAND Characteristics

## 3.1 Performance

| Density | Sequential read (MB/s) | Sequential write (MB/s) | Test condition |
|---|---|---|---|
| **4GB** | 130 | 10 | • Option: Cache / Packed CMD / HS200<br>• Test tool: uBOOT (Without O/S)<br>• Chunk size : 1MB, Test area : 1GB |

## 3.2 Power

### 3.2.1 Active power consumption during operation

| Density | | Icc | Iccq |
|---|---|---|---|
| 4GB(SDP) | Average | 40mA | 100mA |
| | Peak | 80mA | 200mA |

- Room temperature : 25℃
- Average current consumption is over a period of 100ms
- Peak current consumption is over a period of 20us
- $V_{cc}$ : 3.3V & $V_{ccq}$ : 1.8V
- HS200 enabled

### 3.2.2 Low power mode (Standby)

| Density | Icc | Iccq |
|---|---|---|
| 4GB(SDP) | 100uA | 30uA |

- In Standby Power mode, CTRL $V_{ccq}$ & NAND $V_{cc}$ power supply is switched on
- No data transaction period before entering sleep status
- Room temperature : 25℃

### 3.2.3 Low power mode (Sleep)

| Density | Icc | Iccq |
|---|---|---|
| 4GB(SDP) | 0 | 30uA |

- In sleep state, triggered by CMD5, NAND $V_{cc}$ power supply is switched off (CTRL $V_{ccq}$ on)
- Room temperature : 25℃

## 3.3 Endurance

This section provides "TBW(Total Bytes Written)" information that indicates how much data can be written on an e-NAND before the device reaches its end of life.
The data is based on the SK hynix's data pattern which is designed to be a good indication of endurance for mainstream application users.

| Density | TBW |
|---|---|
| **4GB** | 2.4TB |

**[Table 2]Write endurance**

# 4. e-NAND New feature for eMMC4.5

## 4.1 HS200 mode

e-NAND supports HS200 signaling to achieve a bus speed of 200MB/s via a 200MHz SDR clock frequency. HS200 mode supports x4, x8 bit bus width and the 1.8V $V_{ccq}$. e-NAND supports up to 4 Driver Strength.

| Driver type values | Support | Nominal Impedance | Approximated driving capability compared to Type_0 | Remark |
|---|---|---|---|---|
| 0 | Mandatory | 50Ω | x 1 | Default Driver Type.<br>Supports up to 200MHz operation. |
| 1 | Optional | 33Ω | x 1.5 | Supports up to 200MHz operation. |
| 2 | | 66Ω | x 0.75 | The weakest driver that supports up to 200MHz operation. |
| 3 | | 100Ω | x 0.5 | For low noise and low EMI systems.<br>Maximal operating frequency is decided by host design. |

**[Table 3]I/O Driver strength types**

Selecting **HS_Timing** depends on Host I/F speed, default is 0, but all of value can be selected by host.

| Value | Timing | Supportability for e-NAND |
|---|---|---|
| 0x00 | Selecting backward compatibility interface timing | Support |
| 0x01 | High speed | Support |
| 0x02 | HS200 | Support |

**[Table 4]HS_Timing values**

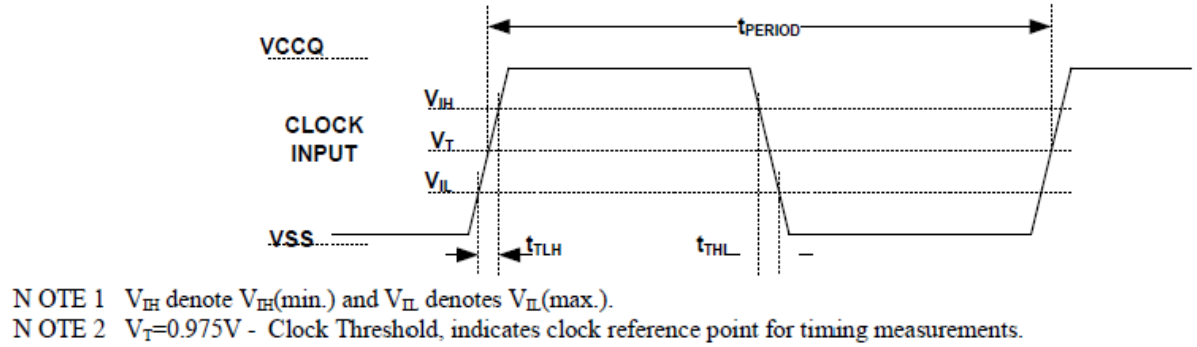
### 4.1.1 Bus timing specification in HS200 mode

**■ HS200 clock timing**

CLK Timing in HS200 mode shall conform to the timing specified in Figure3 and Table 5. CLK input shall satisfy the clock timing over all possible operation and environment conditions.CLK input parameters should be measured while CMD and DAT lines are stable high or low, as close as possible to the Device.
The maximum frequency of HS200 is 200MHz. Hosts can use any frequency up to the maximum that HS200 mode allows.

| Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|
| $t_{PERIOD}$ | 5 | - | ns | 200MHz(Max.), between rising edges |
| $t_{TLH}$, $t_{THL}$ | - | 0.2*$t_{PERIOD}$ | ns | $t_{TLH}$, $t_{THL}$ < 1ns(max) at 200MHz, $C_{BGA}$=12pF, The absolute maximum value of tTLH, tTHL is 10ns regardless of clock frequency. |
| Duty Cycle | 30 | 70 | % | |

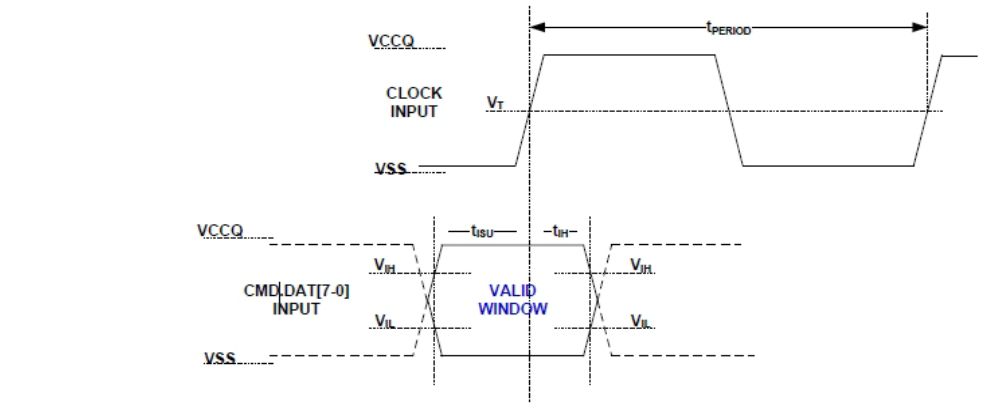
**[Table 5]HS200 clock signal timing**




N OTE 1 $V_{IH}$ denote $V_{IH}$(min.) and $V_{IL}$ denotes $V_{IL}$(max.).
N OTE 2 $V_T$=0.975V - Clock Threshold, indicates clock reference point for timing measurements.

**[Figure 3]HS200 clock signal timing**

## ■ HS200 Device input timing



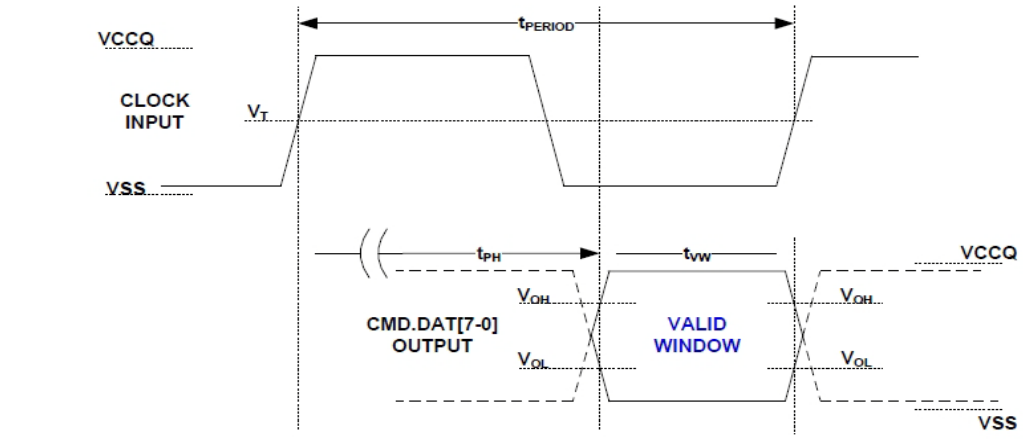

Note1: $t_{ISU}$ and $t_{IH}$ are measured at $V_{IL}$(max.) and $V_{IH}$(min.).
Note2: $V_{IH}$ denote $V_{IH}$(min.) and $V_{IL}$ denotes $V_{IL}$(max.).

**[Figure 4]HS200 Device input timing**

| Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|
| $t_{ISU}$ | 1.40 | - | ns | 5pF≤$C_{BGA}$≤12pF |
| $t_{IH}$ | 0.8 | | ns | 5pF≤$C_{BGA}$≤12pF |

**[Table 6]HS200 Device input timing**

## ■ HS200 Device output timing



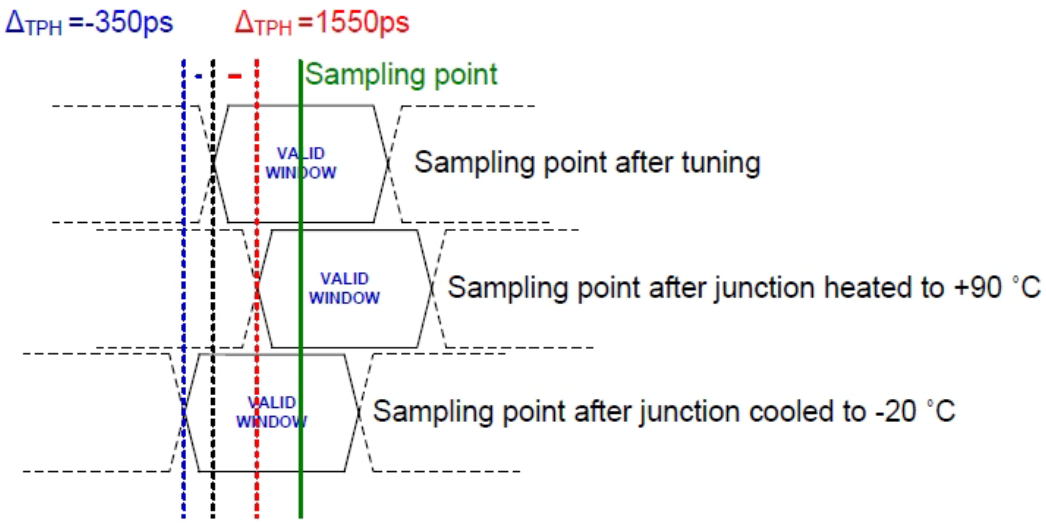

Note: $V_{OH}$ denotes $V_{OH}$(min.) and $V_{OL}$ denotes $V_{OL}$(max.).

**[Figure 5]HS200 Device output timing**

| Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|
| $t_{PH}$ | 0 | 2 | UI | Device outout momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift. |
| $\Delta_{TPH}$ | -350 | +1550 ($\Delta_{TPH}$=90 deg.C) | ps | Delay variation due to temperature change after tuning. Total allowable shift of output valid window (Tvw) from last system Tuning procedure $\Delta_{TPH}$ is 2600ps for ΔT from -25 deg.C to 125 deg.C during operation. |
| $t_{VW}$ | 0.575 | - | UI | tvw=2.88ns at 200MHz<br>Using test circuit in Figure19 including skew among CMD and DAT lines creat by the device. Host path may add Signal Integrity included noise, skews, etc.<br>Expected Tvw at Host input is larger than 0.475UI |

**[Table 7]HS200 Device output timing**

• Note **:** Unit Interval(UI) is one bit nominal time. For example, UI=5ns at 200MHz.

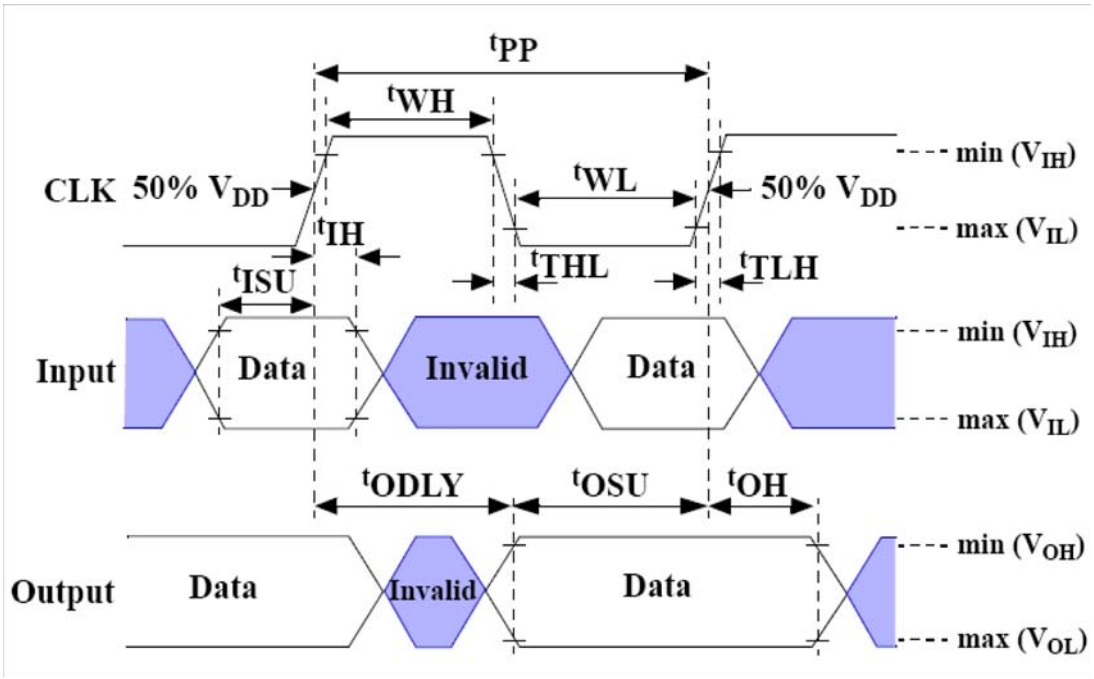



**[Figure 6]$\Delta_{TPH}$ consideration**

# 5. e-NAND general parameters

## 5.1 Timing

### 5.1.1 Bus timing




**Data must always be sampled on the rising edge of the clock.**

**[Figure 7]Timing diagram: data input/output**

| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| **Clock CLK**[1] | | | | | |
| Clock frequency data transfer mode (PP)[2] | $f_{PP}$ | 0 | 52[3] | MHz | $C_L$ ≤30 pF<br>Tolerance: +100KHz |
| Clock frequency identification mode (OD) | $f_{OD}$ | 0 | 400 | kHz | Tolerance: +20KHz |
| Clock high time | $t_{WH}$ | 6.5 | | ns | $C_L$ ≤ 30 pF |
| Clock low time | $t_{WL}$ | 6.5 | | ns | $C_L$ ≤ 30 pF |
| Clock rise time[4] | $t_{TLH}$ | | 3 | ns | $C_L$ ≤ 30 pF |
| Clock fall time | $t_{THL}$ | | 3 | ns | $C_L$ ≤ 30 pF |
| **Inputs CMD, DAT** (referenced to CLK) | | | | | |
| Input set-up time | $t_{ISU}$ | 3 | | ns | $C_L$ ≤ 30 pF |
| Input hold time | $t_{IH}$ | 3 | | ns | $C_L$ ≤ 30 pF |
| **Outputs CMD, DAT** (referenced to CLK) | | | | | |
| Output delay time during data transfer | $t_{ODLY}$ | | 13.7 | ns | $C_L$ ≤ 30 pF |
| Output hold time | $t_{OH}$ | 2.5 | | ns | $C_L$ ≤ 30 pF |
| Signal rise time[5] | $t_{RISE}$ | | 3 | ns | $C_L$ ≤ 30 pF |
| Signal fall time | $t_{FALL}$ | | 3 | ns | $C_L$ ≤ 30 pF |

**[Table 8]High-speed e-NAND interface timing**

- CLK timing is measured at 50% of VDD.
- e-NAND shall support the full frequency range from 0-26Mhz, or 0-52MHz
- CLK rising and falling times are measured by min ($V_{IH}$) and max ($V_{IL}$).
- Input CMD, DAT rising and falling times are measured by min ($V_{IH}$) and max ($V_{IL}$), and output CMD, DAT rising and falingl times are measured by min ($V_{OH}$) and max ($V_{OL}$).

| Parameter | Symbol | Min | Max | Unit | Remark(1) |
|---|---|---|---|---|---|
| **Clock CLK**(2) | | | | | |
| Clock frequency Data Transfer Mode (PP)(3) | $f_{PP}$ | 0 | 26 | MHz | CL ≤ 30 pF |
| Clock frequency Identification Mode (OD) | $f_{OD}$ | 0 | 400 | kHz | |
| Clock high time | $t_{WH}$ | 10 | | ns | CL ≤ 30 pF |
| Clock low time | $t_{WL}$ | 10 | | ns | CL ≤ 30 pF |
| Clock rise time(4) | $t_{TLH}$ | | 10 | ns | CL ≤ 30 pF |
| Clock fall time | $t_{THL}$ | | 10 | ns | CL ≤ 30 pF |
| **Inputs CMD, DAT** (referenced to CLK) | | | | | |
| Input set-up time | $t_{ISU}$ | 3 | | ns | CL ≤ 30 pF |
| Input hold time | $t_{IH}$ | 3 | | ns | CL ≤ 30 pF |
| **Outputs CMD, DAT** (referenced to CLK) | | | | | |
| Output set-up time(5) | $t_{OSU}$ | 11.7 | | ns | CL ≤ 30 pF |
| Output hold time(5) | $t_{OH}$ | 8.3 | | ns | CL ≤ 30 pF |

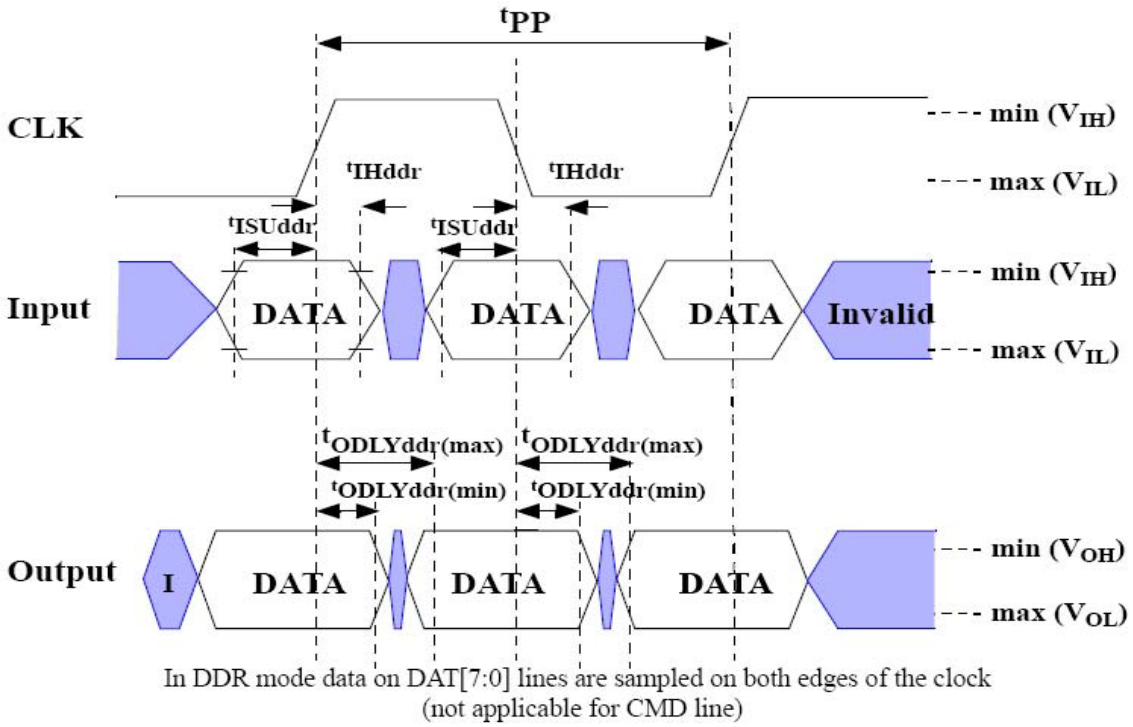
**[Table 9]Backward-compatible e-NAND interface timing**

- e-NAND must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed timing by the host sending the switch command (CMD6) with the argument for high speed interface select.
- CLK timing is measured at 50% of VDD.
- CLK rising and falling times are measured by min ($V_{IH}$) and max ($V_{IL}$).
- $t_{OSU}$ and $t_{OH}$ are defined as values from clock rising edge. However, there may be cards or devices which utilize clock falling edge to output data in backward compatibility mode.

  Therefore, it is recommended for hosts either to set $t_{WL}$ value as long as possible within the range which should not go over $t_{CK}$-$t_{OH}$(min) in the system or to use slow clock frequency, so that host could have data set up margin for those devices. In this case, each device which utilizes clock falling edge might show the correlation either between $t_{WL}$ and $t_{OSU}$ or between $t_{CK}$ and $t_{OSU}$ for the device.

### 5.1.2 Bus timing for DAT signals during 2x data rate operation

These timings apply to the DAT[7:0] signals only when the device is configured for dual data mode operation. In dual data mode, the DAT signals operate synchronously of both the rising and the falling edges of CLK.




**[Figure 8]Timing diagram: data input/output in dual data rate mode**

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| **Input CLK(1)** | | | | | |
| Clock duty cycle | | 45 | 55 | % | Includes jitter, phase noise |
| Clock rise time | $t_{TLH}$ | | 3 | ns | CL≤30 pF |
| Clock fail time | $t_{THL}$ | | 3 | ns | CL≤30 pF |
| **Input CMD (referenced to CLK-SDR mode)** | | | | | |
| Input set-up time | $t_{ISUddr}$ | 3 | | ns | CL≤20 pF |
| Input hold time | $t_{IHDDR}$ | 3 | | ns | CL≤20 pF |
| **Output CMD (referenced to CLK-SDR mode)** | | | | | |
| Output delay time during data transfer | $t_{ODLY}$ | | 13.7 | ns | CL≤20 pF |
| Output hold time | $t_{OH}$ | 2.5 | | ns | CL≤20 pF |
| Signal rise time | $t_{RISE}$ | | 3 | ns | CL≤20 pF |
| Signal fall time | $t_{FALL}$ | | 3 | ns | CL≤20 pF |
| **Input DAT (referenced to CLK-DDR mode)** | | | | | |
| Input set-up time | $t_{ISUddr}$ | 2.5 | | ns | CL≤20 pF |
| Input hold time | $t_{IHddr}$ | 2.5 | | ns | CL≤20 pF |
| **Outputs DAT (referenced to CLK-DDR mode)** | | | | | |
| Output delay time during data transfer | $t_{ODLYddr}$ | 1.5 | 7 | ns | CL≤20 pF |
| Signal rise time(DAT0-7)(2) | $t_{RISE}$ | | 2 | ns | CL≤20 pF |
| Signal fall time (DAT0-7) | $t_{FALL}$ | | 2 | ns | CL≤20 pF |

**[Table 10]Dual data rate interface timings**

- NOTE 1. CLK timing is measured at 50% of VDD.
- NOTE 2. Inputs DAT rising and falling times are measured by min ($V_{IH}$) and max ($V_{IL}$), and outputs CMD, DAT rising and falling times are measured by min ($V_{OH}$) and max ($V_{OL}$)

## 5.2 Bus signal

### 5.2.1 Bus signal line load

The total capacitance $C_L$ of each line of e-MMC bus is the sum of the bus master capacitance $C_{HOST}$, the bus capacitance $C_{BUS}$ itself, and the capacitance $C_{Device}$ of the eMMC connected to this line, and requiring the sum of the host and bus capacitances not to exceed 20 pF.

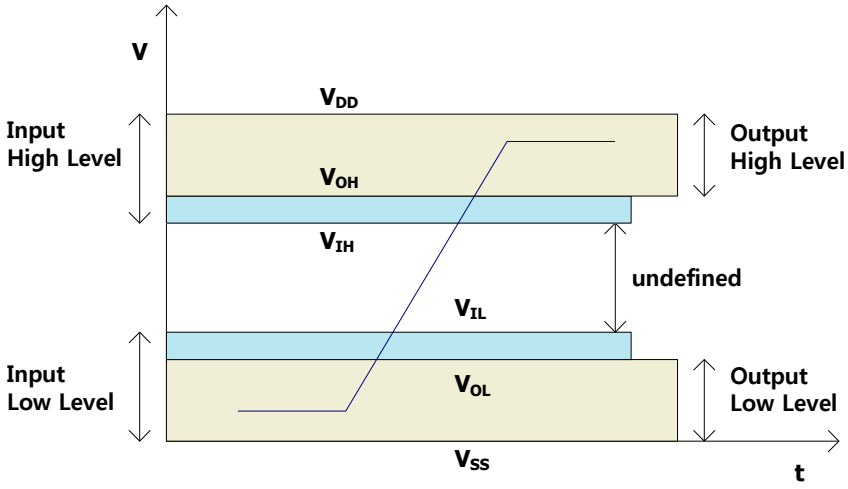
$$C_L = C_{HOST} + C_{BUS} + C_{Device}$$

| Parameter | Symbol | Min | Typ | Max | Unit | Remark |
|---|---|---|---|---|---|---|
| Pull-up resistance for CMD | $R_{CMD}$ | 4.7 | | 100 | Kohm | to prevent bus floating |
| Pull-up resistance for DAT0-7 | $R_{DAT}$ | 10 | | 100 | Kohm | to prevent bus floating |
| Internal pull up resistance DAT1 - DAT7 | $R_{int}$ | 10 | | 150 | Kohm | |
| Bus signal line capacitance | $C_L$ | | | 30 | pF | Single Device |
| Single Device capacitance | $C_{DEVICE}$ | | | 6 | pF | |
| Maximum signal line inductance | | | | 16 | nH | $f_{PP} \leq 52$ MHz |
| VDDi capacitor value | $C_{REG}$ | 0.1 | | | uF | To stabilize regulator output when target device bus speed mode is either backward-compatible, high speed SDR, high speed DDR, or HS200. |
| $V_{ccq}$ decoupling capacitor | $C_{H1}$ | 1 | | | uF | |

**[Table 11]e-NAND capacitance**

### 5.2.3 Bus signal levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.




**[Figure 9]e-NAND bus signal level**

- **Open-Drain mode bus signal level**

| Parameter | Symbol | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $V_{DD}$ - 0.2 | | V | Note[1)] |
| Output low voltage | $V_{OL}$ | | 0.3 | V | $I_{OL}$ = 2mA |

**[Table 12]Open-Drain signal level**

(1) Because $V_{OH}$ depends on external resistance value (including outside the package), this value does not apply as device specification.
Host is responsible to choose the external pull-up and open drain resistance value to meet Voh minimum value.

- **Push-Pull mode bus signal level**

The device input and output voltages shall be within the following specified ranges for any $V_{DD}$ of the allowed voltage range

| Parameter | Symbol | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| Output HIGH voltage | $V_{OH}$ | 0.75 * $V_{ccq}$ | | V | $I_{OH}$ = -100μA @ $V_{ccq}$ min |
| Output LOW voltage | $V_{OL}$ | | 0.125 * $V_{ccq}$ | V | $I_{OL}$ = -100μA @ $V_{ccq}$ min |
| Input HIGH voltage | $V_{IH}$ | 0.625 * $V_{ccq}$ | $V_{ccq}$ + 0.3 | V | |
| Input LOW voltage | $V_{IL}$ | $V_{SS}$ - 0.3 | 0.25 * $V_{ccq}$ | V | |

**[Table 13]Push-Pull signal level 2.7V-3.6V $V_{ccq}$ range**

| Parameter | Symbol | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| Output HIGH voltage | $V_{OH}$ | Vccq - 0.45V | | V | $I_{OH}$ = -2mA |
| Output LOW voltage | $V_{OL}$ | | 0.45V | V | $I_{OL}$ = -2mA |
| Input HIGH voltage | $V_{IH}$ | 0.65 * $V_{ccq}$ | $V_{ccq}$ + 0.3 | V | |
| Input LOW voltage | $V_{IL}$ | $V_{SS}$ - 0.3 | 0.35 * $V_{ccq}$ | V | |

**[Table 14]Push-pull signal level 1.65V-1.95V $V_{ccq}$ range**

## 5.3 Power mode

### 5.3.1 e-NAND power-up guidelines

e-NAND power-up must adhere to the following guidelines:

● When power-up is initiated, either $V_{cc}$ or $V_{ccq}$ can be ramped up first, or both can be ramped up simultaneously.

● After power up, e-NAND enters the pre-idle state. The power up time of each supply voltage should be less than the specified tPRU (tPRUH, tPRUL or tPRUV) for the appropriate voltage range.

● If e-NAND does not support boot mode or its BOOT_PARTITION_ENABLE bit is cleared, e-NAND moves immediately to the idle state. While in the idle state, e-NAND ignores all bus transactions until receiving CMD1.
e-NAND begins boot operation with the argument of 0xFFFFFFFA. If boot acknowledge is finished, e-NAND shall send acknowledge pattern "010" to the host within the specified time. After boot operation is terminated, e-NAND enters the idle state and shall be ready for CMD1 operation. If e-NAND receives CMD1 in the pre-boot state, it begins to respond to the command and moves to the card identification mode.

● When e-NAND is initiated by alternative boot command(CMD0 with arg=0xFFFFFFFA), all the data will be read from the boot partition and then e-NAND automatically goes to idle state, but hosts are still required to issue CMD0 with arg=0x0000000000 in order to complete a boot mode properly and move to the idle state. While in the idle state, e-NAND ignores all bus transactions until it receives CMD1.

● CMD1 is a special synchronization command which is used to negotiate the operating voltage range and poll the device until it is out of its power-up sequence. In addition to the operating voltage profile of the device, the response to CMD1 contains a busy flag indicating that the device is still working on its power-up procedure and is not ready for identification. This bit informs the host that the device is not ready, and the host must wait until this bit is cleared. The device must complete its initialization within 1 second of the first CMD1 issued with a valid OCR range.

● If the e-NAND device was successfully partitioned during the previous power up session (bit 0 of EXT_CSD byte [155] PARTITION_SETTING_COMPLETE successfully set) then the initialization delay is (instead of 1s) calculated from INI_TIMEOUT_PA (EXT_CSD byte [241]). This timeout applies only for the very first initialization after successful partitioning. For all the consecutive initialization 1sec time out will be applied.

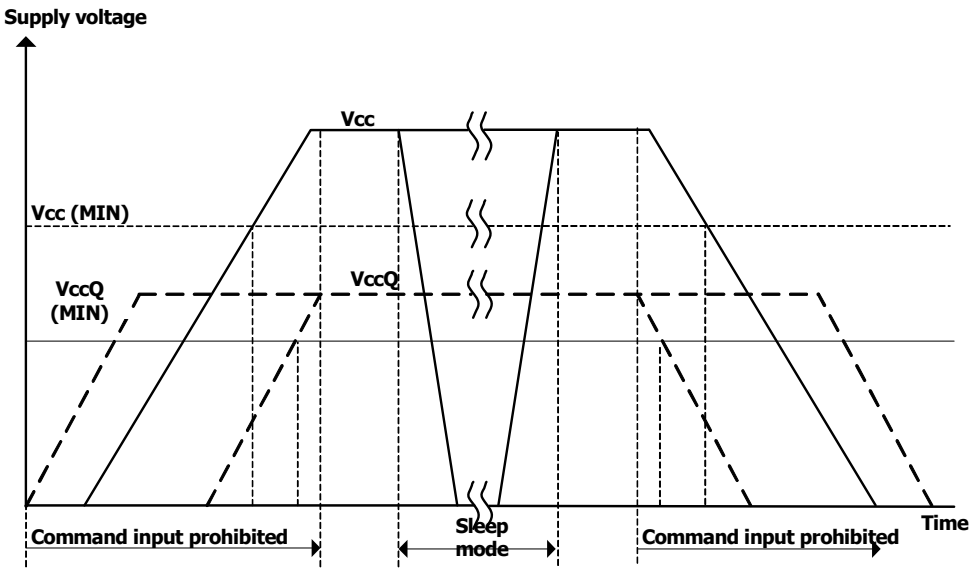
● The bus master moves the device out of the idle state. Because the power-up time and the supply ramp-up time depend on the application parameters such as the bus length and the power supply unit, the host must ensure that power is built up to the operating level (the same level that will be specified in CMD1) before CMD1 is transmitted.

● After power-up, the host starts the clock and sends the initializing sequence on the CMD line. The sequence length is the longest of: 1ms, 74 clocks, the supply ramp-up time, or the boot operation period. An additional 10 clocks (beyond the 64 clocks of the power-up sequence) are provided to eliminate power-up synchronization problems.

● Every bus master must implement CMD1.

### 5.3.2 e-NAND Power Cycling

The master can execute any sequence of $V_{cc}$ and $V_{ccq}$ power-up/power-down. However, the master must not issue any commands until $V_{cc}$ and $V_{ccq}$ are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down $V_{cc}$ to reduce power consumption. It is necessary for the slave to be ramped up to $V_{cc}$ before the host issues CMD5 (SLEEP_AWAKE) to wake the slave unit.




**[Figure 10]e-NAND power cycle**

If $V_{cc}$ or $V_{ccq}$ is below 0.5 V for longer than 1 ms, the slave shall always return to the pre-idle state, and perform the appropriate boot behavior. The slave will behave as in a standard power up condition once the voltages have returned to their functional ranges.
An exception to this behavior is if the device is in sleep state, in which the voltage on $V_{cc}$ is not monitored.

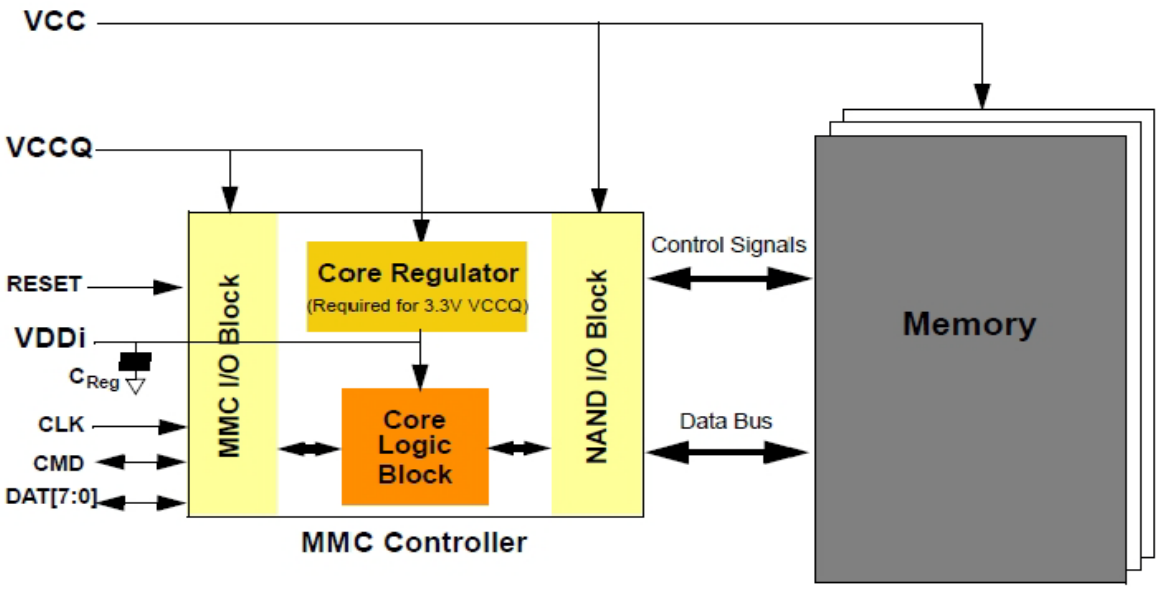
### 5.3.3 Leakage

| Parameter | | Symbol | Min | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| | BGA | | -0.5 | $V_{ccq}$+0.5 | V | |
| **All inputs** | | | | | | |
| Input leakage current (before initialization sequenceand/or the internal-pull up resistors connected) | | | -100 | 100 | μA | |
| Input leakage current (after initialization sequence and the internal pull up resistors disconnected) | | | -2 | 2 | μA | |
| **All outputs** | | | | | | |
| Output leakage current (before initialization sequence) | | | -100 | 100 | μA | |
| Output leakage current (after initialization sequence) | | | -2 | 2 | μA | |

**[Table 15]General operation conditions**

### 5.3.4 Power Supply

In e-NAND, $V_{cc}$ is used for the NAND core voltage and NAND interface; $V_{ccq}$ is for the controller core and e-NAND interface voltage shown in Figure 11. The core regulator is optional and only required when internal core logic voltage is regulated from $V_{ccq}$. A Creg capacitor must be connected to the VDDi terminal to stabilize regulator output on the system.




**[Figure 11]e-NAND internal power diagram**

e-NAND supports one or more combinations of $V_{cc}$ and $V_{ccq}$ as shown in Table 16.
The available voltage configuration is shown in Table 17.

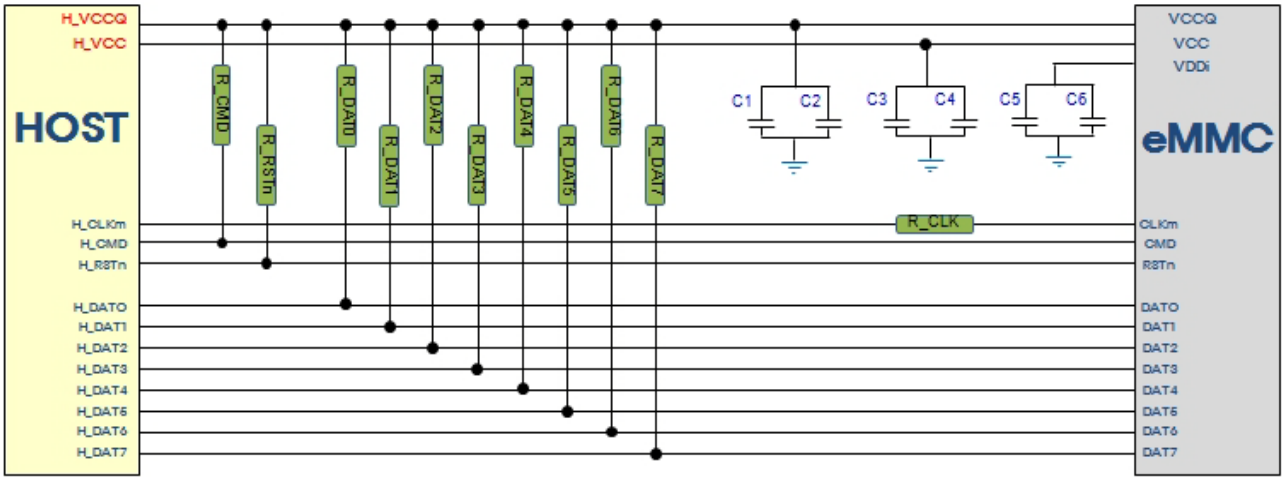
| Parameter | Symbol | Min | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Supply voltage (NAND) | $V_{cc}$ | 2.7 | 3.6 | V | |
| | | 1.7 | 1.95 | V | **Not supported** |
| Supply voltage (I/O) | $V_{ccq}$ | 2.7 | 3.6 | V | |
| | | 1.7 | 1.95 | V | |
| Supply power-up for 3.3V | $t_{PRUH}$ | | 35 | ms | |
| Supply power-up for 1.8V | $t_{PRUL}$ | | 25 | ms | |

**[Table 16]e-NAND power supply voltage**

| | | $V_{ccq}$ | |
|---|---|---|---|
| | | **1.7V ~ 1.95V** | **2.7V ~ 3.6V** |
| **$V_{cc}$** | **2.7V–3.6V** | Valid | Valid |
| | **1.7V–1.95V** | Not Valid | Not Valid |

**[Table 17]e-NAND voltage combinations**

## 5.4 Connection Guide




**[Figure 12]Connection guide drawing**

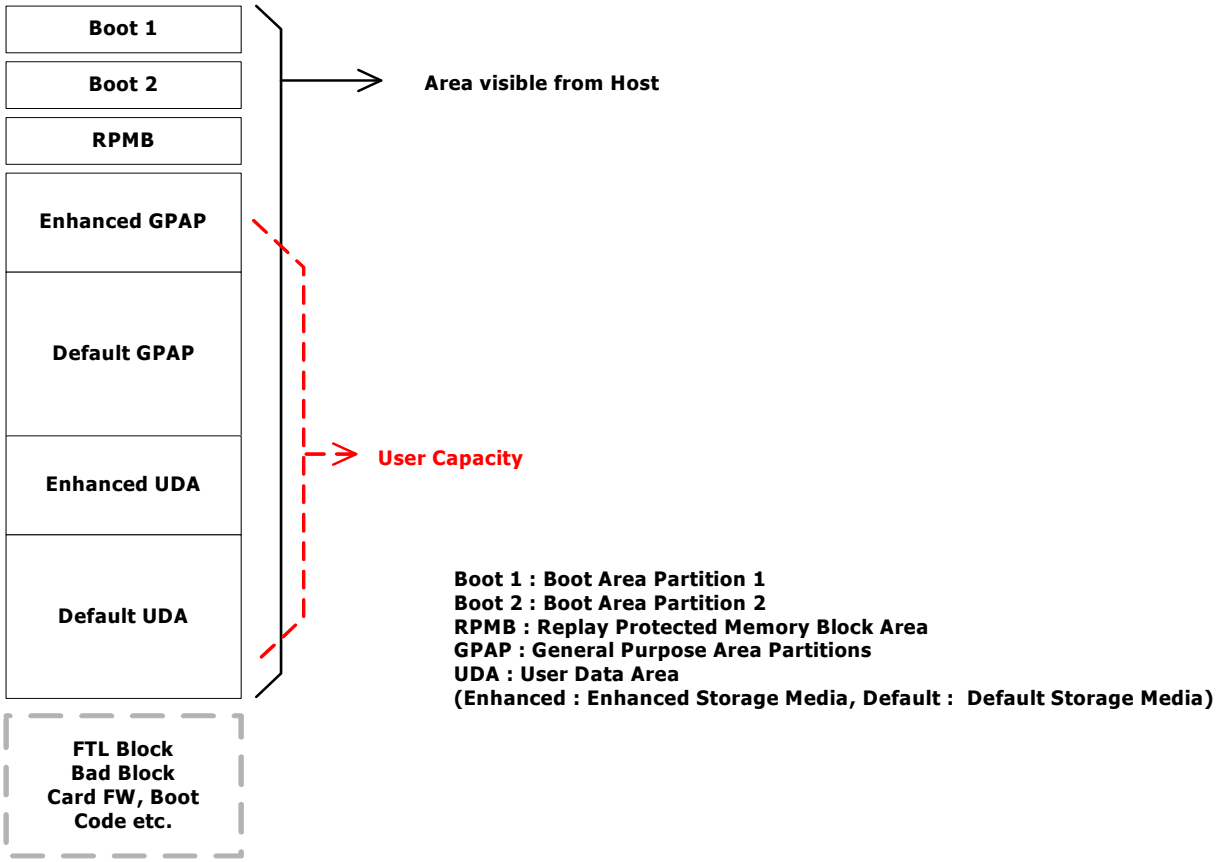
| Parameter | Symbol | Min | Max | Recommend | Unit | Remark |
|---|---|---|---|---|---|---|
| Pull-up resistance for CMD | R_CMD | 4.7 | 100 | 10 | kohm | Pull-up resistance should be put on CMD line to prevent bus floating. |
| Pull-up resistance for DAT0~7 | R_DAT | 10 | 100 | 50 | kohm | Pull-up resistance should be put on DAT line to prevent bus floating. |
| Pull-up resistance for RSTn | R_RSTn | 10 | 100 | 50 | kohm | It is not necessary to put pull-up resistance on RSTn line if host does not use H/W reset. (Extended CSD register [162] = 0b) |
| Serial resistance on CLK | R_CLK | 0 | 30 | 27 | ohm | To reduce overshooting/undershooting<br>Note: If the host uses HS200, we recommend to remove this resister for better CLK signal |
| $V_{ccq}$ capacitor value | C1 & C2 | 2±0.22 | 4.7 | 2.2±0.22 | uF | Coupling cap should be connected with $V_{ccq}$ and Vssqm as closely possible. |
| $V_{cc}$ capacitor value(≤8GB) | C3 & C4 | 4.7±0.47 | 10 | 4.7±0.47 | uF | Coupling cap should be connected with $V_{cc}$ and Vssm as closely possible.<br>$V_{cc}$ /$V_{ccq}$ cap. value would be up to Host requirement and the application system characteristics. |
| $V_{CC}$ capacitor value(>8GB) | | | | | | |
| VDDi capacitor value | C5 & C6 | 0 | 2.2 | 0.1 | uF | Coupling cap should be connected with VDDi and Vssq as closely possible.<br>(Internal Cap : 1uF) |

**[Table 18]Connection guide specification**

# 6. e-NAND basic operations

## 6.1 Partitioning

### 6.1.1 User density




**[Figure 13]Partition diagram**

**■ Boot partition size**

| Density | Boot Partition 1,2 |
|---|---|
| **4GB** | 4096KB |

**■ User density size**

| Capacity | LBA(Hex) | LBA(Dec) | Capacity(Bytes) |
|---|---|---|---|
| **4GB** | 748000h | 7,634,944 | 3,909,091,328 |

- 1sector=512 bytes.
- The total usable capacity of the e-NAND may be less than total physical capacity because a small portion of the capacity is used for NAND flash management and maintenance purpose.

■ **Maximum enhanced partition size**

Enhanced user data area can be configured to store read-centric data such as sensitive data or for other host usage models.
SK hynix e-NAND supports Enhanced User Data Area as SLC Mode. When customer adopts some portion as enhanced user data area in User Data Area, that area occupies double the size of the original set-up size.

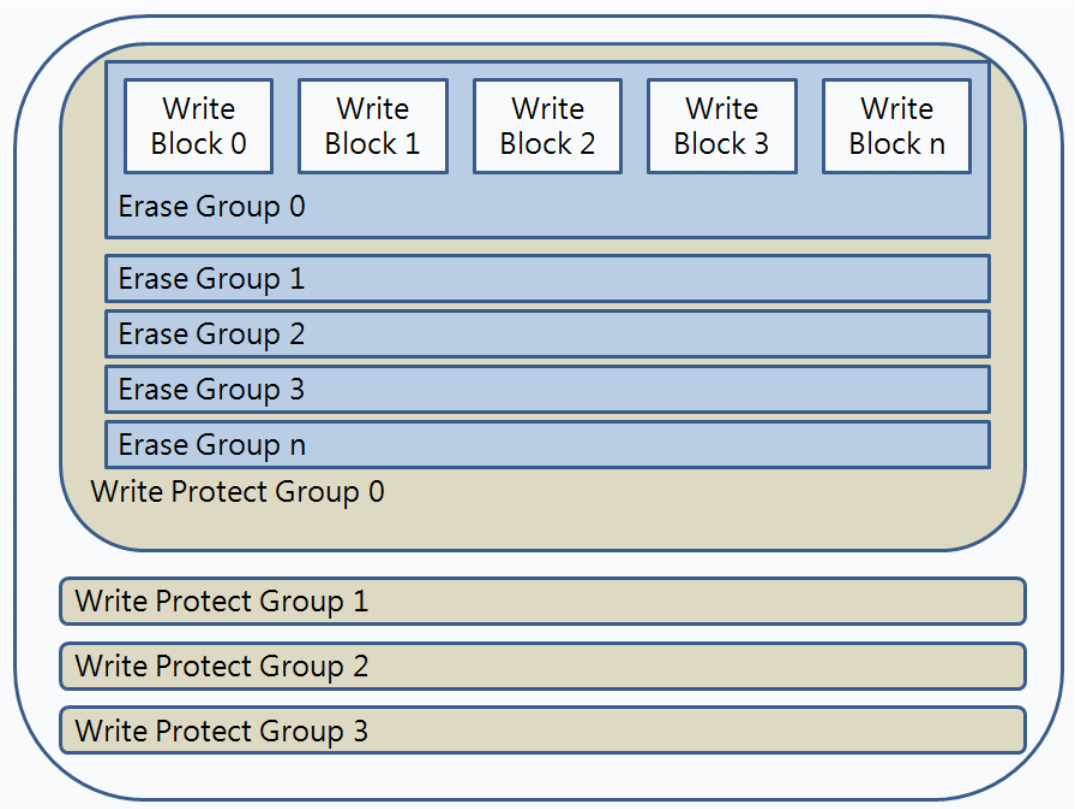
| Capacity | Max ENH_SIZE_MULTI | HC_ERASE_GRP_SIZE | HC_WP_GRP_SIZE |
|---|---|---|---|
| **4GB** | E9h | 1h | 10h |

- 1sector = 512 bytes.

Max Enhanced Partition Size is defined as **MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512Byte.**

| Capacity | LBA(Hex) | LBA(Dec) | Capacity(Bytes) |
|---|---|---|---|
| **4GB** | 3A4000h | 3,817,472 | 1,954,545,664 |

### 6.1.2 Erase / Write protect group size

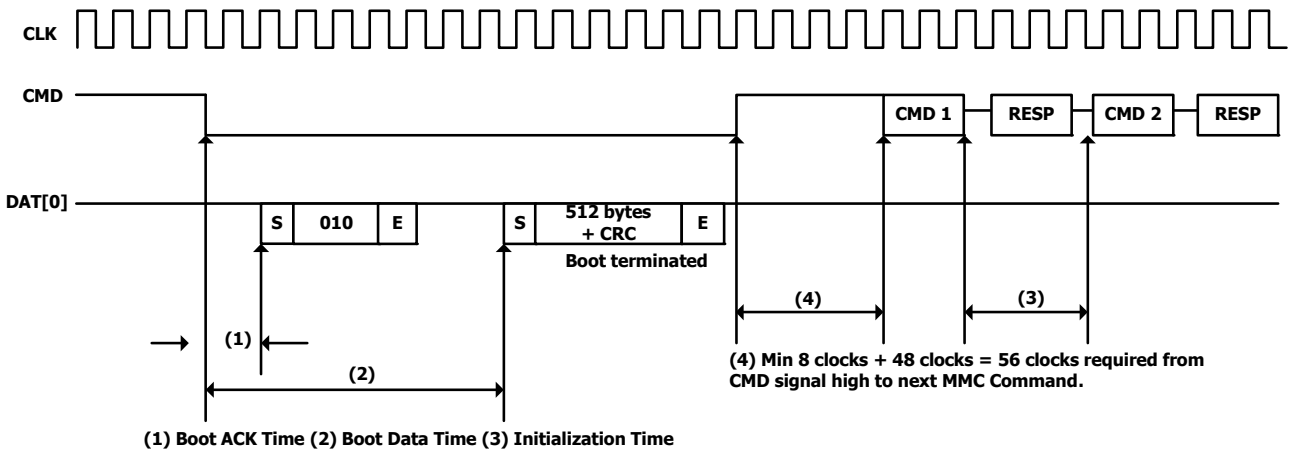



| Density | Erase group size | | Write protect group size |
|---|---|---|---|
| | ERASE_GROUP_DEF=0 | ERASE_GROUP_DEF=1 | |
| 4GB | 512KB | 512KB | 8MB |

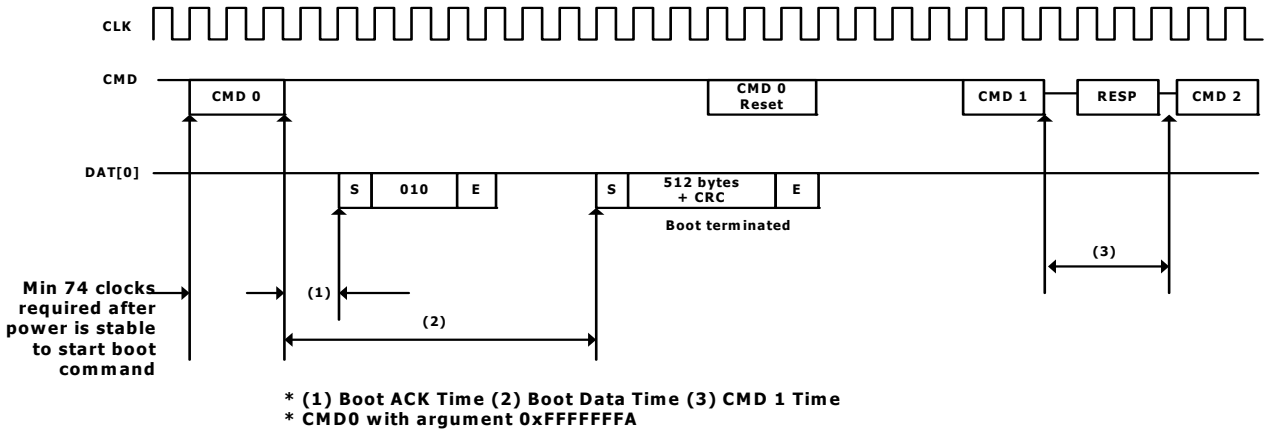
**[Table 19]Erase / Write protect Group size**

## 6.2 Boot operation

e-NAND supports boot mode and alternative boot mode. e-NAND also, supports high speed timing and dual data rate during boot.




**[Figure 14]e-NAND state diagram (Boot mode)**




**[Figure 15]e-NAND state diagram (Alternative boot mode)**

| Timing Factor | Value |
|---|---|
| (1) Boot ACK Time | < 50 ms |
| (2) Boot Data Time | < 1 sec |
| (3) Initialization Time | < 1 sec |

- Initialization time includes partition setting, Please refer to INI_TIMEOUT_AP in Extended CSD Register. Initialization time is completed within 1sec from issuing CMD1 until receiving response.
- The device has to send the acknowledge pattern "010" to the master within 50ms after the CMD0 with the argument of 0xFFFFFFFA is received.

## 7. Time out

| Timing parameter | Value | Remark |
|---|---|---|
| Read timeout | Max 100ms | |
| Write timeout<br>(CMD to write Done) | Max 500ms | |
| Erase timeout | Max 50 ms | Erase group size : 512KB |
| Force erase timeout | Max 3 min | |
| Discard timeout | Max 600ms | |
| Trim timeout | Max 400ms | |
| Secure trim | Max 6s | Unmapping only |
| Sanitize | 8min | |
| Secure erase | Max 6s | Unmapping only |
| Initialization timeout | Max 1s | CMD to Response |
| 1st Initialization timeout after partitioning | Max 1s | BOOT1/2, RPMB, UDA & EUDA |
| PON busy Time (Short / Long) | Max 100ms / 1s | PON long busy time includes garbage collection time. |
| Initialization after PON (Short / Long) | 180ms~580ms | |
| BKOP exit time by HPI | Max 100ms | BKOP off time after HPI |
| Auto-BKOP exit Time | Max 100ms | BKOP off time after any CMD from host |
| HPI | Max 100ms | Response after HPI |
| CMD5 sleep In | 2ms | |

**[Table 20]Time out value**

- eMMC I/F : HS200
- Pre-conditioning states - Clean state / Test Range : Random write - 1GB, Random read - 1GB
- Sequential read / write chunk size : 1MB
- Current numbers are based on aligned 4KB
- SKhynix recommends to erase all blocks before sanitize operation to shorten the sanitize time

# 8. Device registers

There are six different registers within the device interface:

- Operation conditions register (OCR)
- Card identification register (CID)
- Card specific data register (CSD)
- Relative card address register (RCA)
- DSR (Driver Stage Register)
- Extended card specific data register (EXT_CSD).

These registers are used for the serial data communication and can be accessed only using the corresponding commands.
e-NAND has a status register to provide information about the current device state and completion codes for the last host command.

## 8.1 Operation conditions register (OCR)

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of e-NAND and the access mode indication. In addition, this register includes a status information bit. This status bit is set if e-NAND power up procedure has been finished.

| OCR bit | Description | SK hynix e-NAND |
|---|---|---|
| [6:0] | Reserved | 000 0000b |
| [7] | 1.70 - 1.95V | 1b |
| [14:8] | 2.0 - 2.6 | 000 0000b |
| [23:15] | 2.7 - 3.6 (High $V_{ccq}$ range) | 1111 1111 1b |
| [28:24] | Reserved | 000 000b |
| [30:29] | Access mode | 10b (sector mode) |
| [31] | (card power up status bit (busy))(1) | |

**[Table 21]OCR register definition**

1) This bit is set to LOW if the card has not finished the power up routine

## 8.2 Card identification (CID) register

The card identification (CID) register is 128 bits wide. It contains e-NAND identification information used during e-NAND identification phase (e-NAND protocol). Every individual e-NAND has a unique identification number. The structure of the CID register is defined in the following sections.

| Name | Field | Width | CID slice | CID value | Remark |
|---|---|---|---|---|---|
| Manufacturer ID | MID | 8 | [127:120] | 90h | |
| Reserved | | 6 | [119:114] | | |
| Card/BGA | CBX | 2 | [113:112] | 01h | BGA |
| OEM/application ID | OID | 8 | [111:104] | 4Ah | |
| Product name | PNM | 48 | [103:56] | 4GB: 483447326111h | |
| Product revision | PRV | 8 | [55:48] | 01h | |
| Product serial number | PSN | 32 | [47:16] | - | Not Fixed |
| Manufacturing date | MDT | 8 | [15:8] | - | Not Fixed |
| CRC7 checksum | CRC | 7 | [7:1] | - | Not Fixed |
| Not used, always '1' | Reserved | 1 | [0:0] | 1 | |

**[Table 22]Card identification (CID) fields**

## 8.3 Card specific data register (CSD)

The card specific data (CSD) register provides information on how to access e-NAND contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed and so on. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the CSD Registry entries in the Table 23 below is coded as follows:

- ***R:*** Read only.
- ***W:*** One time programmable and not readable.
- ***R/W:*** One time programmable and readable.
- ***W/E:*** Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
- ***R/W/E:*** Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
- ***R/W/C_P:*** Writable after value cleared by power failure and HW/rest assertion (the value not cleared by CMD0 reset) and readable.
- ***R/W/E_P:*** Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
- ***W/E_P:*** Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

| Name | Field | Width | Cell type | CSD slice | CSD value | Remark |
|---|---|---|---|---|---|---|
| CSD structure | CSD_STRUCTURE | 2 | R | [127:126] | 3h | |
| System specification version | SPEC_VERS | 4 | R | [125:122] | 4h | |
| Reserved | | 2 | R | [121:120] | | |
| Data read access-time 1 | TAAC | 8 | R | [119:112] | 27h | |
| Data read access-time 2 in CLK cycles (NSAC*100) | NSAC | 8 | R | [111:104] | 1h | |
| Max. bus clock frequency | TRAN_SPEED | 8 | R | [103:96] | 32h | |
| Card command classes | CCC | 12 | R | [95:84] | F5h | |
| Max. read data block length | READ_BL_LEN | 4 | R | [83:80] | 9h | |
| Partial blocks for read allowed | READ_BL_PARTIAL | 1 | R | [79:79] | 0h | |
| Write block misalignment | WRITE_BLK_MISALIGN | 1 | R | [78:78] | 0h | |
| Read block misalignment | READ_BLK_MISALIGN | 1 | R | [77:77] | 0h | |
| DSR implemented | DSR_IMP | 1 | R | [76:76] | 0h | |
| Reserved | | 2 | R | [75:74] | | |
| Device size | C_SIZE | 12 | R | [73:62] | FFFh | |
| Max. read current @ VDD min | VDD_R_CURR_MIN | 3 | R | [61:59] | 7h | |
| Max. read current @ VDD max | VDD_R_CURR_MAX | 3 | R | [58:56] | 7h | |
| Max. write current @ VDD min | VDD_W_CURR_MIN | 3 | R | [55:53] | 7h | |
| Max. write current @ VDD max | VDD_W_CURR_MAX | 3 | R | [52:50] | 7h | |
| Device size multiplier | C_SIZE_MULT | 3 | R | [49:47] | 7h | |
| Erase group size | ERASE_GRP_SIZE | 5 | R | [46:42] | 1Fh | |
| Erase group size multiplier | ERASE_GRP_MULT | 5 | R | [41:37] | 1Fh | |
| Write protect group size | WP_GRP_SIZE | 5 | R | [36:32] | Fh | |
| Write protect group enable | WP_GRP_ENABLE | 1 | R | [31:31] | 1h | |
| Manufacturer default ECC | DEFAULT_ECC | 2 | R | [30:29] | 0h | |
| Write speed factor | R2W_FACTOR | 3 | R | [28:26] | 2h | |
| Max. write data block length | WRITE_BL_LEN | 4 | R | [25:22] | 9h | |
| Partial blocks for write allowed | WRITE_BL_PARTIAL | 1 | R | [21:21] | 0h | |
| Reserved | | 4 | R | [20:17] | | |
| Content protection application | CONTENT_PROT_APP | 1 | R | [16:16] | 0h | |
| File format group | FILE_FORMAT_GRP | 1 | R/W | [15:15] | 0h | |
| Copy flag (OTP) | COPY | 1 | R/W | [14:14] | 1h | |
| Permanent write protection | PERM_WRITE_PROTECT | 1 | R/W | [13:13] | 0h | |
| Temporary write protection | TMP_WRITE_PROTECT | 1 | R/W/E | [12:12] | 0h | |
| File format | FILE_FORMAT | 2 | R/W | [11:10] | 0h | |
| ECC code | ECC | 2 | R/W/E | [9:8] | 0h | |
| CRC | CRC | 7 | R/W/E | [7:1] | 69h | |

**[Table 23]CSD fields (continued)**

The following sections describe the CSD fields and the relevant data types. If not explicitly defined otherwise, all bit strings are interpreted as binary coded numbers starting with the left bit first.

## 8.4 Extended CSD register

The Extended CSD register defines e-NAND properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines e-NAND capabilities and cannot be modified by the host. The lower 192 bytes are the modes segment, which defines the configuration e-NAND is working in. These modes can be changed by the host by means of the switch command.

| Name | Field | CSD slice | Cell Type | EXT_CSD value | Remark |
|---|---|---|---|---|---|
| **Properties segment** | | | | | |
| Reserved | | [511:506] | | | |
| Extended Security Commands Error | EXT_SECURITY_ERR | [505] | R | 0h | |
| Supported command sets | S_CMD_SET | [504] | R | 1h | |
| HPI features | HPI_FEATURES | [503] | R | 3h | |
| Background operation support | BKOPS_SUPPORT | [502] | R | 1h | |
| Max packed read commands | MAX_PACKED_READS | [501] | R | 8h | |
| Max packed write commands | MAX_PACKED_WRITES | [500] | R | 8h | |
| Data Tag Support | DATA_TAG_SUPPORT | [499] | R | 1h | |
| Tag Unit Size | TAG_UNIT_SIZE | [498] | R | 0h | |
| Tag Resources Size | TAG_RES_SIZE | [497] | R | 6h | |
| Context management capabilities | CONTEXT_CAPABILITIES | [496] | R | 78h | |
| Large Unit size | LARGE_UNIT_SIZE_M1 | [495] | R | 1h | |
| Extended partitions attribute support | EXT_SUPPORT | [494] | R | 3h | |
| Reserved | | [493:253] | | | |
| Cache size | CACHE_SIZE | [252:249] | R | 200h | |
| Generic CMD6 timeout | CENERIC_CMD6_TIME | [248] | R | 64h | |
| Power off notification(long)timeout | POWER_OFF_LONG_TIME | [247] | R | 64h | |
| Background operations status | BKOPS_STATUS | [246] | R | 0h | |
| Number of correctly programmed sectors | CORRECTLY_PRG_SECTORS_NUM | [245:242] | R | 0h | |
| 1st initialization time after partitioning | INI_TIMEOUT_AP | [241] | R | 0Ah | |
| Reserved | | [240] | | | |
| Power class for 52MHz, DDR at 3.6V | PWR_CL_DDR_52_360 | [239] | R | 0h | |
| Power class for 52MHz, DDR at 1.95V | PWR_CL_DDR_52_195 | [238] | R | 0h | |
| Power class for 200MHz at 1.95V | PWR_CL_200_195 | [237] | R | 0h | |
| Power class for 200MHz at 1.3V | PWR_CL_200_130 | [236] | R | 0h | |

**[Table 24]Extended CSD**

| Name | Field | CSD slice | Cell Type | EXT_CSD value | Remark |
|---|---|---|---|---|---|
| Minimum write performance for 8bit at 52MHz in DDR mode | MIN_PERF_DDR_W_8_52 | [235] | R | 0h | |
| Minimum read performance for 8bit at 52MHz in DDR mode | MIN_PERF_DDR_R_8_52 | [234] | R | 0h | |
| Reserved | | [233] | | | |
| TRIM multiplier | TRIM_MULT | [232] | R | 2h | |
| Secure feature support | SEC_FEATURE_SUPPORT | [231] | R | 55h | |
| Secure erase multiplier | SEC_ERASE_MULT | [230] | R | Ah | |
| Secure TRIM multiplier | SEC_TRIM_MULT | [229] | R | Ah | |
| Boot information | BOOT_INFO | [228] | R | 7h | |
| Reserved | | [227] | | | |
| Boot partition size | BOOT_SIZE_MULTI | [226] | R | 20h | |
| Access size | ACC_SIZE | [225] | R | 6h | |
| High-capacity erase unit size | HC_ERASE_GRP_SIZE | [224] | R | 1h | |
| High_capacity erase timeout | ERASE_TIMEOUT_MULT | [223] | R | 2h | |
| Reliable write sector count | REL_WR_SEC_C | [222] | R | 10h | |
| High-capacity write protect group size | HC_WP_GRP_SIZE | [221] | R | 4GB:10h | 8 high-capacity erase unit size |
| Sleep current(VCC) | S_C_VCC | [220] | R | 7h | |
| Sleep current(VCCQ) | S_C_VCCQ | [219] | R | 7h | |
| Reserved | | [218] | | | |
| Sleep/awake timeout | S_A_TIMEOUT | [217] | R | 13h | |
| Reserved | | [216] | | | Reserved |
| Sector count | SEC_COUNT | [215:212] | R | 4GB : 748000h | Sector count |
| Reserved | | [211] | | | Reserved |
| Minimum write performance for 8bit at52MHz | MIN_PERF_W_8_52 | [210] | R | 8h | Minimum write performance for 8bit at52MHz |
| Minimum read performance for 8bit at 52MHz | MIN_PERF_R_8_52 | [209] | R | 8h | Minimum read performance for 8bit at 52MHz |
| Minimum write performance for 8bit at 26MHz, for 4bit at 52MHz | MIN_PERF_W_8_26_4_52 | [208] | R | 8h | Minimum write performance for 8bit at 26MHz, for 4bit at 52MHz |
| Minimum read performance for 8bit at 26MHz, for 4bit at 52MHz | MIN_PERF_R_8_26_4_52 | [207] | R | 8h | Minimum read performance for 8bit at 26MHz, for 4bit at 52MHz |
| Minimum write performance for 4bit at 26MHz | MIN_PERF_W_4_26 | [206] | R | 8h | Minimum write performance for 4bit at 26MHz |

**[Table 24]Extended CSD**

| Name | Field | CSD slice | Cell Type | EXT_CSD value | Remark |
|---|---|---|---|---|---|
| Minimum read performance for 4bit at 26MHz | MIN_PERF_R_4_26 | [205] | R | 8h | |
| Reserved | | [204] | | | |
| Power class for 26MHz at 3.6V | PWR_CL_26_360 | [203] | R | 0h | |
| Power class for 52MHz at 3.6V | PWR_CL_52_360 | [202] | R | 0h | |
| Power class for 26MHz at 1.95V | PWR_CL_26_195 | [201] | R | 0h | |
| Power class for 52MHz at 1.95V | PWR_CL_52_195 | [200] | R | 0h | |
| Partition switching timing | PARTITION_SWITCH_TIME | [199] | R | 3h | |
| Out-of-interrupt busy timing | OUT_OF_INTERRUPT_TIME | [198] | R | 5h | |
| I/O Driver Strength | DRIVER_STRENGTH | [197] | R | 1h | |
| Device type | DEVICE_TYPE | [196] | R | 17h | |
| Reserved | | [195] | | | |
| CSD structure version | CARD_STRUCTURE | [194] | R | 2h | |
| Reserved | | [193] | | | |
| Extended CSD revision | EXT_CSD_REV | [192] | R | 6h | |
| **Modes Segment** | | | | | |
| Command set | CMD_SET | [191] | R/W/E_P | 0h | |
| Reserved | | [190] | | | |
| Command set revision | CMD_SET_REV | [189] | R | 0h | |
| Reserved | | [188] | | | |
| Power class | POWER_CLASS | [187] | R/W/E_P | 0h | See EXT_CSD in spec. |
| Reserved | | [186] | | | |
| High-speed interface timing | HS_TIMING | [185] | R/W/E_P | 1h | |
| Reserved | | [184] | | | |
| Bus width mode | BUS_WIDTH | [183] | W/E_P | 2h | |
| Reserved | | [182] | | | |
| Erased memory content | ERASED_MEM_CONT | [181] | R | 0h | Erased memory range shall be '0' |
| Reserved | | [180] | | | |
| Partition configuration | PARTITION_CONFIG | [179] | R/W/E & R/ WE_P | 0h | See EXT_CSD in spec |
| Boot config protection | BOOT_CONFIG_PROT | [178] | R/W & R/W/ C_P | 0h | See EXT_CSD in spec |
| Boot bus width | BOOT_BUS_WIDTH | [177] | R/W/E | 0h | See EXT_CSD in spec |
| Reserved | | [176] | | | |

**[Table 24]Extended CSD**

| Name | Field | CSD slice | Cell Type | EXT_CSD value | Remark |
|---|---|---|---|---|---|
| High-density erase group definition | ERASE_GROUP_DEF | [175] | R/W/E_P | 0h | |
| Reserved | | [174] | | | |
| Boot area write protection register | BOOT_WP | [173] | R/W & R/W/C_P | 0h | |
| Reserved | | [172] | | | |
| User area write protection register | USER_WP | [171] | R/W,R/W/C_P & R/W/E_P | 0h | |
| Reserved | | [170] | | | |
| FW configuration | FW_CONFIG | [169] | R/W | 0h | |
| RPMB Size | RPMB_SIZE_MULT | [168] | R | 20h | |
| Write reliability setting register | WR_REL_SET | [167] | R/W | 1Fh | |
| Write reliability parameter register | WR_REL_PARAM | [166] | R | 5h | |
| Sanitize start | SANITIZE_START | [165] | W/E_P | 0h | - |
| Manually start background operations | BKOPS_START | [164] | W/E_P | 0h | |
| Enable background operations handshake | BKOPS_EN | [163] | R/W | 0h | |
| H/W reset function | RST_n_FUNCTION | [162] | R/W | 0h | |
| HPI management | HPI_MGMT | [161] | R/W/E_P | 0h | |
| Partitioning support | PARTITIONING_SUPPORT | [160] | R | 7h | |
| Max enhanced area size | MAX_ENH_SIZE_MULT | [159:157] | R | 4GB : E9h | |
| Partitions attribute | PARTITIONS_ATTRIBUTE | [156] | R/W | 0h | |
| Paritioning setting | PARTITION_SETTING_COMPLETED | [155] | R/W | 0h | |
| General purpose partition size | GP_SIZE_MULT | [154:143] | R/W | 0h | |
| Enhanced user data area size | ENH_SIZE_MULT | [142:140] | R/W | 0h | |
| Enhanced user data start address | ENH_START_ADDR | [139:136] | R/W | 0h | |
| Reserved | | [135] | | | |
| Bad Block management mode | SEC_BAD_BLK_MGMNT | [134] | R/W | 0h | |
| Reserved | | [133] | | | |
| Package Case Temperature is controlled | TCASE_SUPPORT | [132] | W/E_P | 0h | |
| Periodic Wake-up | PERIODIC_WAKEUP | [131] | R/W/E | 0h | |
| Program CID/CSD in DDR mode support | PROGRAM_CID_CSD_DDR_SUPPORT | [130] | R | 0h | |
| Reserved | | [129:128] | | | |

**[Table 24]Extended CSD**

| Name | Field | CSD slice | Cell Type | EXT_CSD value | Remark |
|---|---|---|---|---|---|
| Vendor Specific Fields | VENDOR_SPECIFIC_FIELD | [127:64] | Vendor Specific | - | |
| Native sector size | NATIVE_SECTOR_SIZE | [63] | R | 1h | |
| Sector size emulation | USE_NATIVE_SECTOR | [62] | R/W | 0h | |
| Sector size | DATA_SECTOR_SIZE | [61] | R | 0h | |
| 1st initialization after disabling sector size emulation | INI_TIMEOUT_EMU | [60] | R | 0Ah | |
| Class 6 commands control | Class6_CTRL | [59] | R/W/E_P | 0h | |
| Number of addressed group to be Released | DYNCAP_NEEDED | [58] | R | 0h | |
| Exception events control | EXCEPTION_EVENTS_CTRL | [57:56] | R/W/E_P | 0h | |
| Exception events status | EXCEPTION_EVENTS_STATUS | [55:54] | R | 0h | |
| Extended Partitions Attribute | EXT_PARTITIONS_ATTRIBUTE | [53:52] | R/W | 0h | |
| Context configuration | CONTEXT_CONF | [51:37] | R/W/E_P | 0h | |
| Packed command status | PACKED_COMMAND_STATUS | [36] | R | 0h | |
| Packed command failure index | PACKED_FAILURE_INDEX | [35] | R | 0h | |
| Power Off Notification | POWER_OFF_NOTIFICATION | [34] | R/W/E_P | 0h | |
| Control to turn the Cache ON/ OFF | CACHE_CTRL | [33] | R/W/E_P | 0h | |
| Flushing of the cache | FLUSH_CACHE | [32] | W/E_P | 0h | |
| Reserved | | [31:0] | TBD | | |
| Context configuration | CONTEXT_CONF | [51:37] | R/W/E_P | 0h | |
| Packed command status | PACKED_COMMAND_STATUS | [36] | R | 0h | |
| Packed command failure index | PACKED_FAILURE_INDEX | [35] | R | 0h | |

**[Table 24]Extended CSD**

- Reserved bits should read as "0"
- Obsolete values should be don't care

## 8.5 RCA (Relative card address)

The writable 16-bit relative card address (RCA) register carries the card address assigned by the host during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7.

## 8.6 DSR (Driver stage register)

It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of Devices). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.