8-BIT PARALLEL-LOAD SHIFT REGISTERS

FEATURES

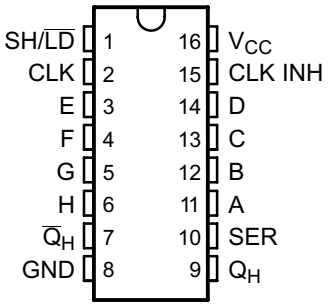
- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 80-μA Max I_{CC}**
- **Typical t_{pd} = 13 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**

DESCRIPTION

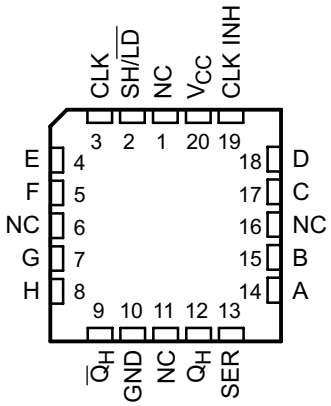
The ’HC165 devices are 8-bit parallel-load shift registers that, when clocked, shift the data toward a serial (Q_H) output. Parallel-in access to each stage is provided by eight individual direct data (A−H) inputs that are enabled by a low level at the shift/load (SH/$\overline{LD}$) input. The ’HC165 devices also feature a clock-inhibit (CLK INH) function and a complementary serial ($\overline{Q}$H) output.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/LD is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. While SH/$\overline{LD}$ is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

SN54HC165 . . . J or W PACKAGE
SN74HC165 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC165 . . . FK PACKAGE
(TOP VIEW)



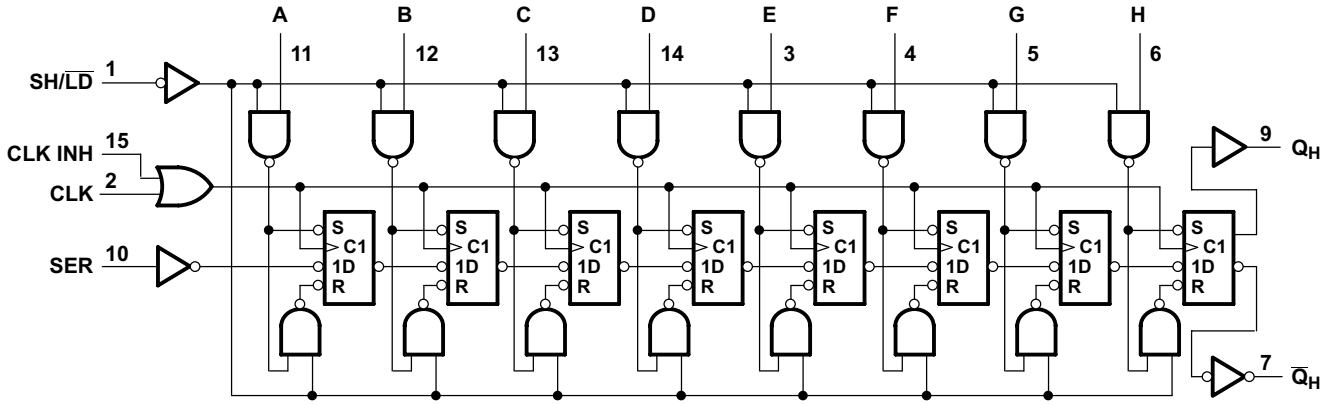
NC − No internal connection

FUNCTION TABLE

INPUTS			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	L	↑	Shift(1)
H	↑	L	Shift(1)

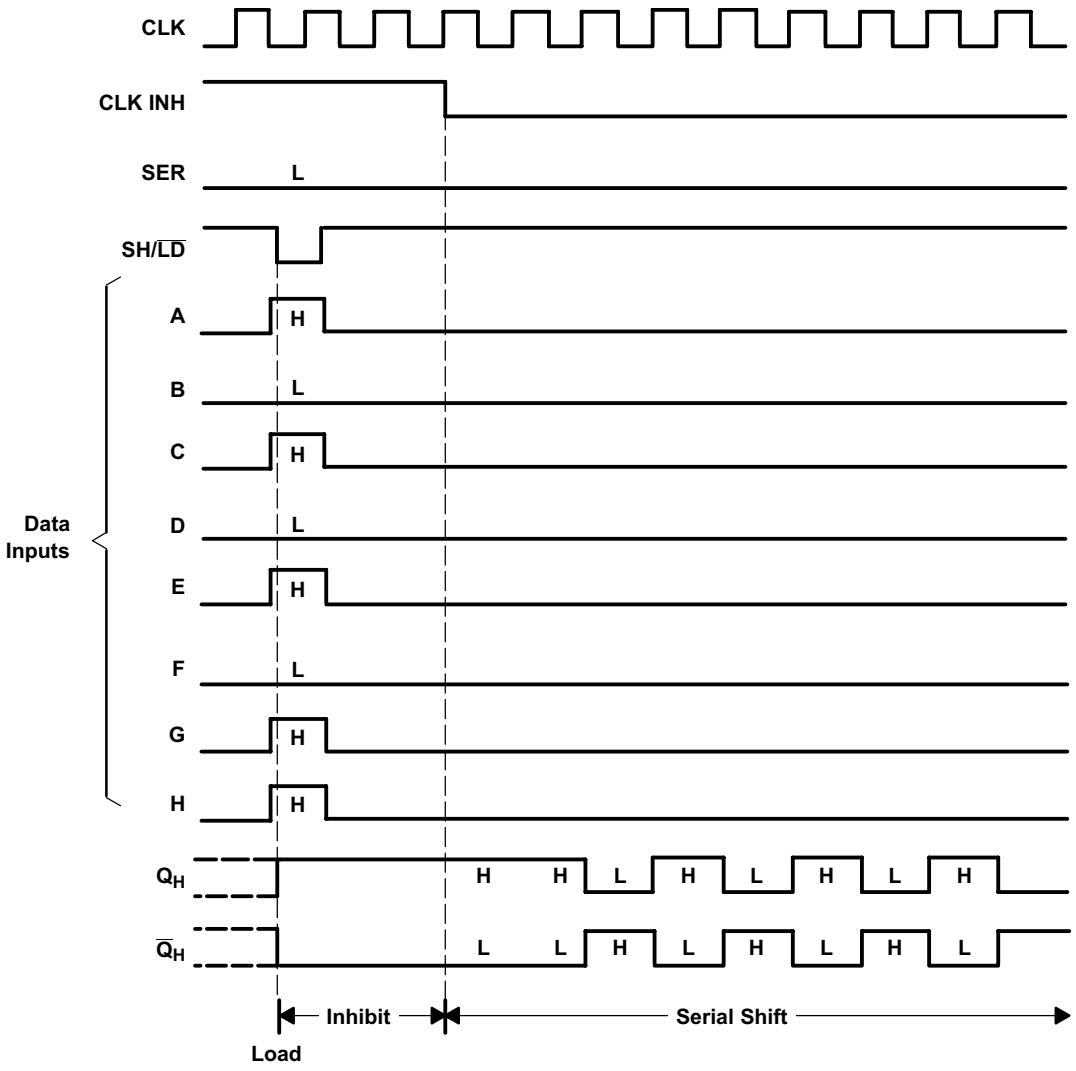
(1) Shift = content of each internal register shifts toward serial output Q_H. Data at SER is shifted into the first register.

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

TYPICAL SHIFT, LOAD, AND INHIBIT SEQUENCE



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNITS
V_{CC}	Supply voltage range		−0.5 to 7	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{CC}$(2)	±20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$(2)	±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}	±25	mA
	Continuous current through V_{CC} or GND		±50	mA
θ_{JA}(3)	Package thermal impedance	D package	73	°C/W
		DB Package	82	°C/W
		N package	67	°C/W
		NS package	64	°C/W
		PW package	108	°C/W
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

over operating free-air temperature range (unless otherwise noted)

			SN54HC165			SN74HC165			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low level input voltage	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$(2)	Input transition rise/fall time	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5 V			500			500	
		V_{CC} = 6 V			400			400	
T_A	Operating free-air temperature		−55		125	−40		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) If this device is used in the threshold region (from V_{IL} max = 0.5 V to V_{IH} min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC165 −55°C TO 125°C		SN74HC165 −40°C TO 85°C		Recommended SN74HC165 −40°C TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		5.9		
		I_{OH} = −4 mA	4.5 V	3.98	4.3		3.7		3.84		3.7		
		I_{OH} = −5.2 mA	6 V	5.48	5.8		5.2		5.34		5.2		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1	0.1			0.1		0.1	V
			4.5 V		0.001	0.1	0.1			0.1		0.1	
			6 V		0.001	0.1	0.1			0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26	0.4			0.33		0.4	
		I_{OL} = 5.2 mA	6 V		0.15	0.26	0.4			0.33		0.4	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100	±1000			±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8	160			80		160	μA
C_i			2 V to 6 V		3	10	10			10		10	pF

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC165 –55°C TO 125°C		SN74HC165 –40°C TO 85°C		Recommended SN74HC165 –40°C TO 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V		6		4.2		5		4.2	MHz
			4.5 V		31		21		25		21	
			6 V		36		25		29		25	
t_w	Pulse duration	SH/$\overline{LD}$ low	2 V	80		120		100		120		ns
			4.5 V	16		24		20		24		
			6 V	14		20		17		20		
		CLK high or low	2 V	80		120		100		120		
			4.5 V	16		24		20		24		
			6 V	14		20		17		20		
t_{su}	Setup time	SH/$\overline{LD}$ high before CLK↑	2 V	80		120		100		120		ns
			4.5 V	16		24		20		24		
			6 V	14		20		17		20		
		SER before CLK↑	2 V	40		60		50		60		
			4.5 V	8		12		10		12		
			6 V	7		10		9		10		
		CLK INH low before CLK↑	2 V	100		150		125		150		
			4.5 V	20		30		25		30		
			6 V	17		25		21		25		
		CLK INH high before CLK↑	2 V	40		60		50		60		
			4.5 V	8		12		10		12		
			6 V	7		10		9		10		
		Data before SH/$\overline{LD}$↓	2 V	100		150		125		150		ns
			4.5 V	20		30		25		30		
			6 V	17		26		21		26		
t_h	Hold time	SER data after CLK↑	2 V	5		5		5		5		ns
			4.5 V	5		5		5		5		
			6 V	5		5		5		5		
		PAR data after SH/$\overline{LD}$↓	2 V	5		5		5		5		
			4.5 V	5		5		5		5		
			6 V	5		5		5		5		

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 3)

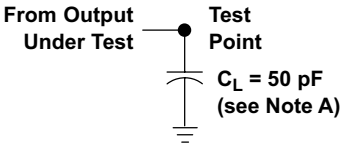
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC165 –55°C TO 125°C		SN74HC165 –40°C TO 85°C		Recommended SN74HC165 –40°C TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	13		4.2		5		4.2		MHz
			4.5 V	31	50		21		25		21		
			6 V	36	62		25		29		25		
t_{pd}	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$	2 V		80	150		225		190		225	ns
			4.5 V		20	30		45		38		45	
			6 V		16	26		38		32		38	
	CLK	Q_H or $\overline{Q}_H$	2 V		75	150		225		190		225	
			4.5 V		15	30		45		38		45	
			6 V		13	26		38		32		38	
	H	Q_H or $\overline{Q}_H$	2 V		75	150		225		190		225	
			4.5 V		15	30		45		38		45	
			6 V		13	26		38		32		38	
t_t		Any	2 V		38	75		110		95		110	ns
			4.5 V		8	15		22		19		22	
			6 V		6	13		19		16		19	

OPERATING CHARACTERISTICS

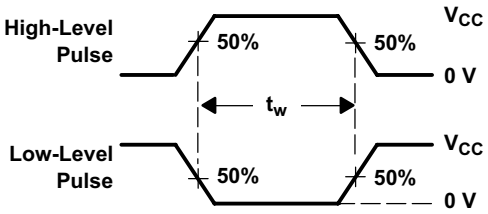
T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	75	pF

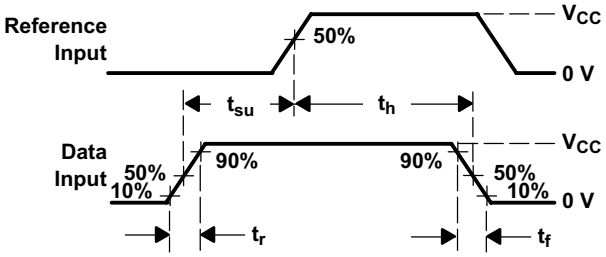
PARAMETER MEASUREMENT INFORMATION



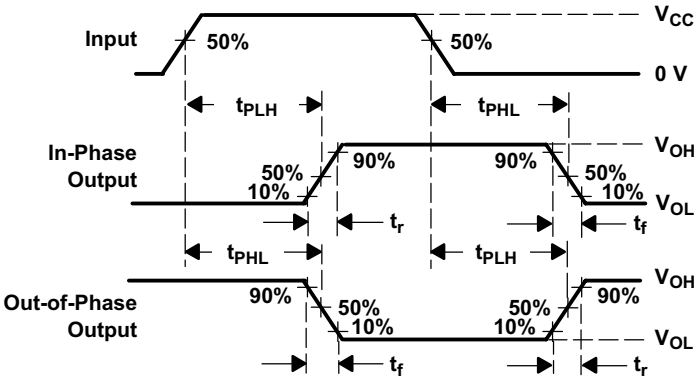
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms