74ABT574A

Octal D-type flip-flop; 3-state

Rev. 2 — 23 November 2012 Product data sheet

1. General description

The 74ABT574A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT574A is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The clock input (CP) and output enable input ($\overline{OE}$) control gates, control the two sections of the device independently. The state of each data input (Dn, one set-up time before the Low-to-High clock transition) is transferred to the Q output of the corresponding flip-flop.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance “off” state, which means they do not drive or load the bus.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the clock operation.

2. Features and benefits

- 74ABT574A is flow-through pinout version of 74ABT374A
- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State outputs for bus interfacing
- Power-on 3-state
- Power-on reset
- Common output enable
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Live insertion/extraction permitted.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT574AN	–40 °C to +85 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74ABT574AD	–40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ABT574ADB	–40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74ABT574APW	–40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram

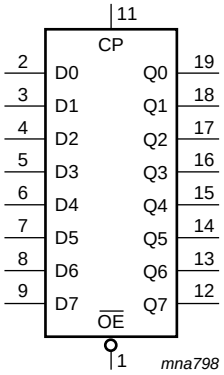


Fig 1. Logic symbol

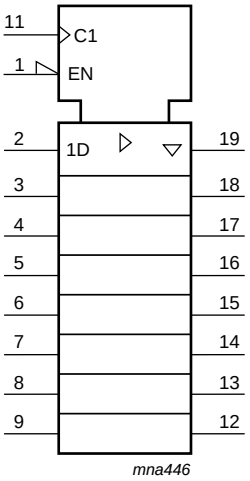


Fig 2. IEC logic symbol

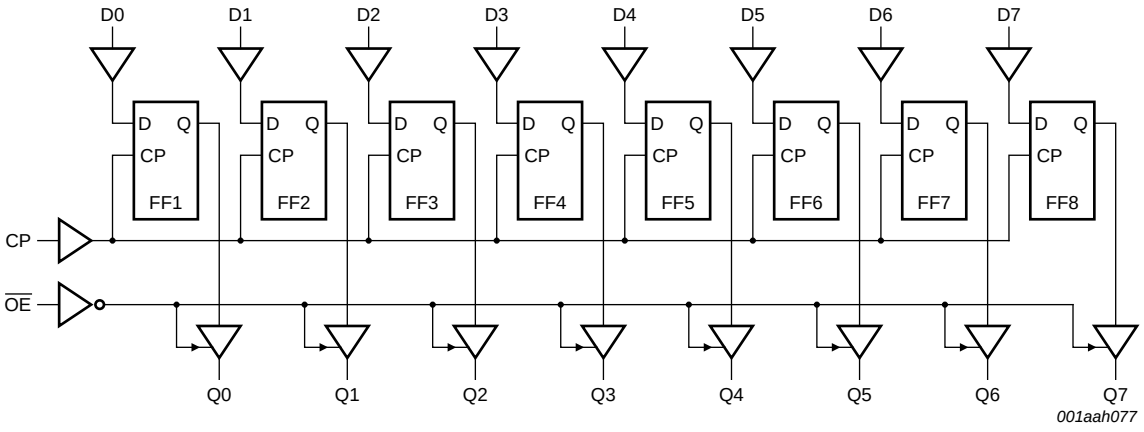


Fig 3. Logic diagram

5. Pinning information

5.1 Pinning

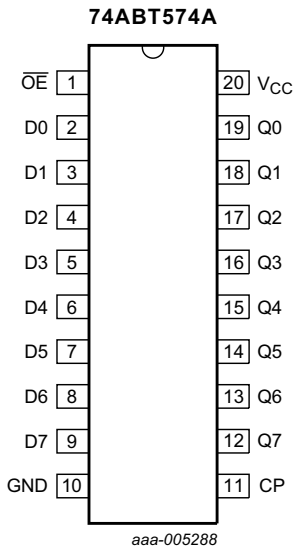


Fig 4. Pin configuration DIP20 and SO20

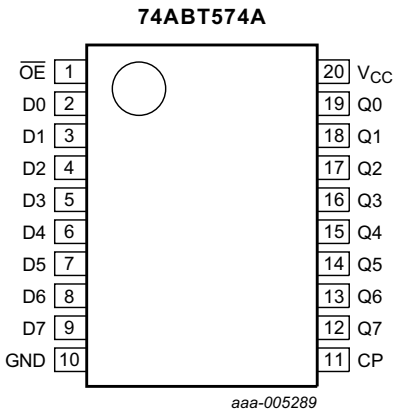


Fig 5. Pin configuration SSOP20 and TSSOP20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	3-state output enable input (active LOW)
D0, D1, D2, D3, D4, D5, D6, D7	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
CP	11	clock pulse input (active rising edge)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	19, 18, 17, 16, 15, 14, 13, 12	3-state flip-flop output
V_{CC}	20	supply voltage

6. Functional description

Table 3. Function table[1]

Operating mode	Input			Internal flip-flop	Output
	$\overline{OE}$	CP	Dn		Qn
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable output	H	↑	l	L	Z
	H	↑	h	H	Z

[1] H = HIGH voltage level;
h = HIGH voltage level one setup time before the HIGH-to-LOW CP transition;
L = LOW voltage level;
l = LOW voltage level one setup time before the HIGH-to-LOW CP transition;
Z = high-impedance OFF-state;
↑ = LOW-to-HIGH clock transition.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage		[1]	–1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1]	–0.5	+5.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–18	-	mA
I_{OK}	output clamping current	$V_O < 0$ V		–50	-	mA
I_O	output current	output in LOW-state		-	128	mA
T_j	junction temperature		[2]	-	150	°C
T_{stg}	storage temperature			–65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		–32	-	-	mA

Table 5. Operating conditions *...continued*

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OL}	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	5	ns/V
T_{amb}	ambient temperature	in free air	−40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions		25 °C			−40 °C to +85 °C		Unit
				Min	Typ	Max	Min	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_{IK} = −18 mA		−1.2	−0.9	-	−1.2	-	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IL}$ or V_{IH}							
		V_{CC} = 4.5 V; I_{OH} = −3 mA		2.5	2.9	-	2.5	-	V
		V_{CC} = 5.0 V; I_{OH} = −3 mA		3.0	3.4	-	3.0	-	V
		V_{CC} = 4.5 V; I_{OH} = −32 mA		2.0	2.4	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; $V_I = V_{IL}$ or V_{IH}		-	0.42	0.55	-	0.55	V
$V_{OL(pu)}$	power-up LOW-level output voltage	V_{CC} = 5.5 V; I_O = 1 mA; V_I = GND or V_{CC}	[1]	-	0.13	0.55	-	0.55	V
I_I	input leakage current	V_{CC} = 5.5 V; $V_I = V_{CC}$ or GND		-	±0.01	±1.0	-	±1.0	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or $V_O \leq$ 4.5 V		-	±5.0	±100	-	±100	µA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} = 2.0 V; V_O = 0.5 V; V_I = GND or V_{CC}; $\overline{OE}$ HIGH	[2]	-	±5.0	±50	-	±50	µA
I_{OZ}	OFF-state output current	V_{CC} = 5.5 V; $V_I = V_{IL}$ or V_{IH}							
		V_O = 2.7 V		-	5.0	50	-	50	µA
		V_O = 0.5 V		−50	−5.0	-	−50	-	µA
I_{LO}	output leakage current	HIGH-state; V_O = 5.5 V; V_{CC} = 5.5 V; V_I = GND or V_{CC}		-	5.0	50	-	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V	[3]	−180		−40	−180	−40	mA
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}							
		outputs HIGH-state		-	100	250	-	250	µA
		outputs LOW-state		-	24	30	-	30	mA
		outputs disabled		-	100	250	-	250	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 5.5 V; one input at 3.4 V; other inputs at V_{CC} or GND	[4]	-	0.5	1.5	-	1.5	mA

Table 6. Static characteristics *…continued*

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
C_I	input capacitance	V_I = 0 V or V_{CC}	-	3	-	-	-	pF
C_O	output capacitance	outputs disabled; V_O = 0 V or V_{CC}	-	6	-	-	-	pF

[1] For valid test results, do not load data into the flip-flops (or latches) after applying the power.

[2] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. A transition time of up to 100 μs is permitted between V_{CC} = 2.1 V and V_{CC} = 5 V ± 10 %.

[3] Do not test more than one output at a time, and the duration of the test must not exceed one second.

[4] This characteristic is the increase in supply current for each input at 3.4 V.

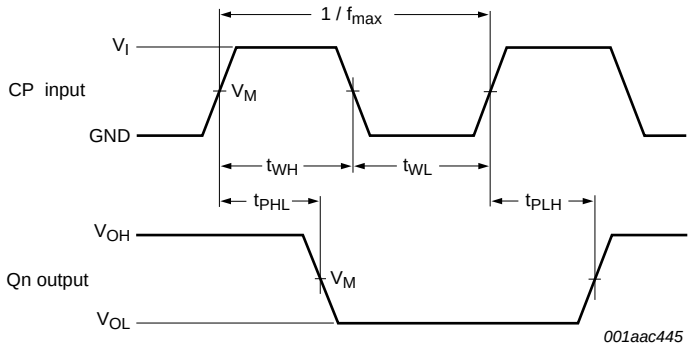
10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; for test circuit, see Figure 9.

Symbol	Parameter	Conditions	25 °C; V_{CC} = 5.0 V			–40 °C to +85 °C; V_{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
f_{max}	maximum frequency	see Figure 6	150	400	-	125	-	MHz
t_{PLH}	LOW to HIGH propagation delay	CP to Qn, see Figure 6	1.5	3.0	4.4	1.5	5.0	ns
t_{PHL}	HIGH to LOW propagation delay	CP to Qn, see Figure 6	2.0	3.4	4.7	2.0	5.1	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{OE}$ to Qn; see Figure 8	1.0	2.9	4.1	1.0	5.0	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{OE}$ to Qn; see Figure 8	2.5	3.8	5.2	2.5	5.7	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OE}$ to Qn; see Figure 8	1.8	3.1	4.3	1.8	5.0	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OE}$ to Qn; see Figure 8	1.4	2.6	3.8	1.4	4.0	ns
$t_{su(H)}$	set-up time HIGH	Dn to CP; see Figure 7	1.0	0.6	-	1.0	-	ns
$t_{su(L)}$	set-up time LOW	Dn to CP; see Figure 7	1.0	0.2	-	1.0	-	ns
$t_{h(H)}$	hold time HIGH	CP to Dn; see Figure 7	+1.0	–0.7	-	1.0	-	ns
$t_{h(L)}$	hold time LOW	CP to Dn; see Figure 7	+1.0	–0.4	-	1.0	-	ns
t_{WH}	pulse width HIGH	CP; see Figure 6	2.0	0.7	-	2.0	-	ns
t_{WL}	pulse width LOW	CP; see Figure 6	2.0	0.8	-	2.0	-	ns

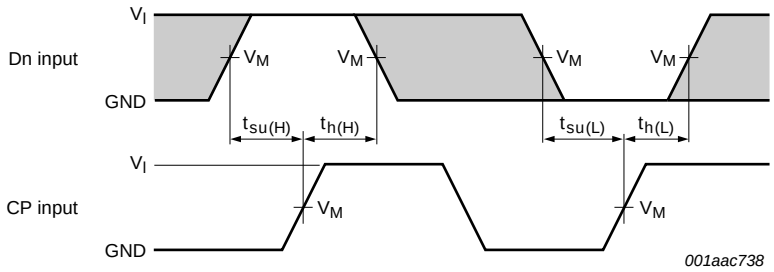
11. Waveforms



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

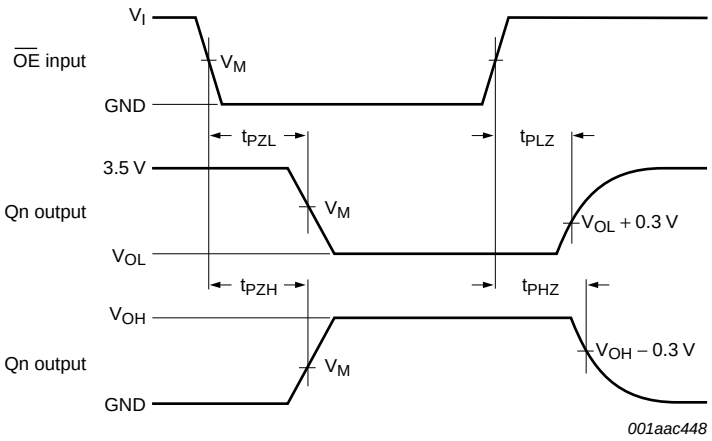
Fig 6. Propagation delay clock input (CP) to output (Qn), clock pulse (CP) width and maximum clock (CP) frequency



V_M = 1.5 V

The shaded areas indicate when the input is permitted to change for predictable output performance.

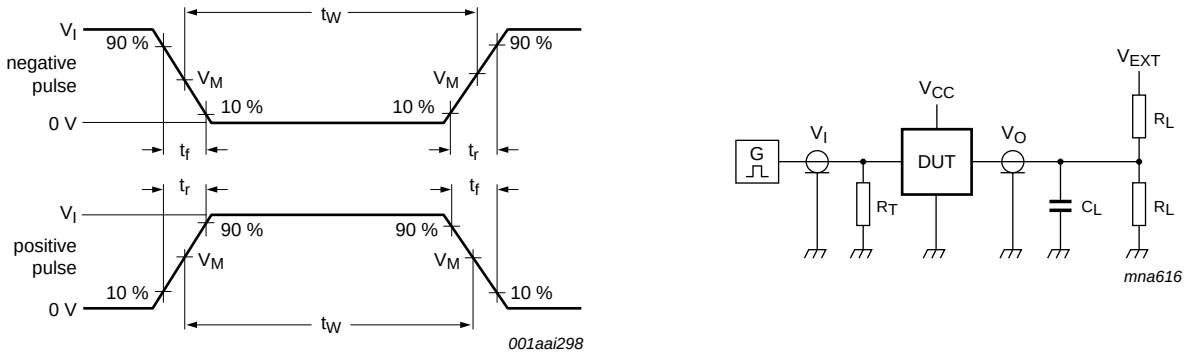
Fig 7. Set-up and hold times data output (Dn) to clock (CP)



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load

Fig 8. 3-state output (Qn) enable and disable times



a. Input pulse definition

b. Test circuit

Test data is given in Table 8.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

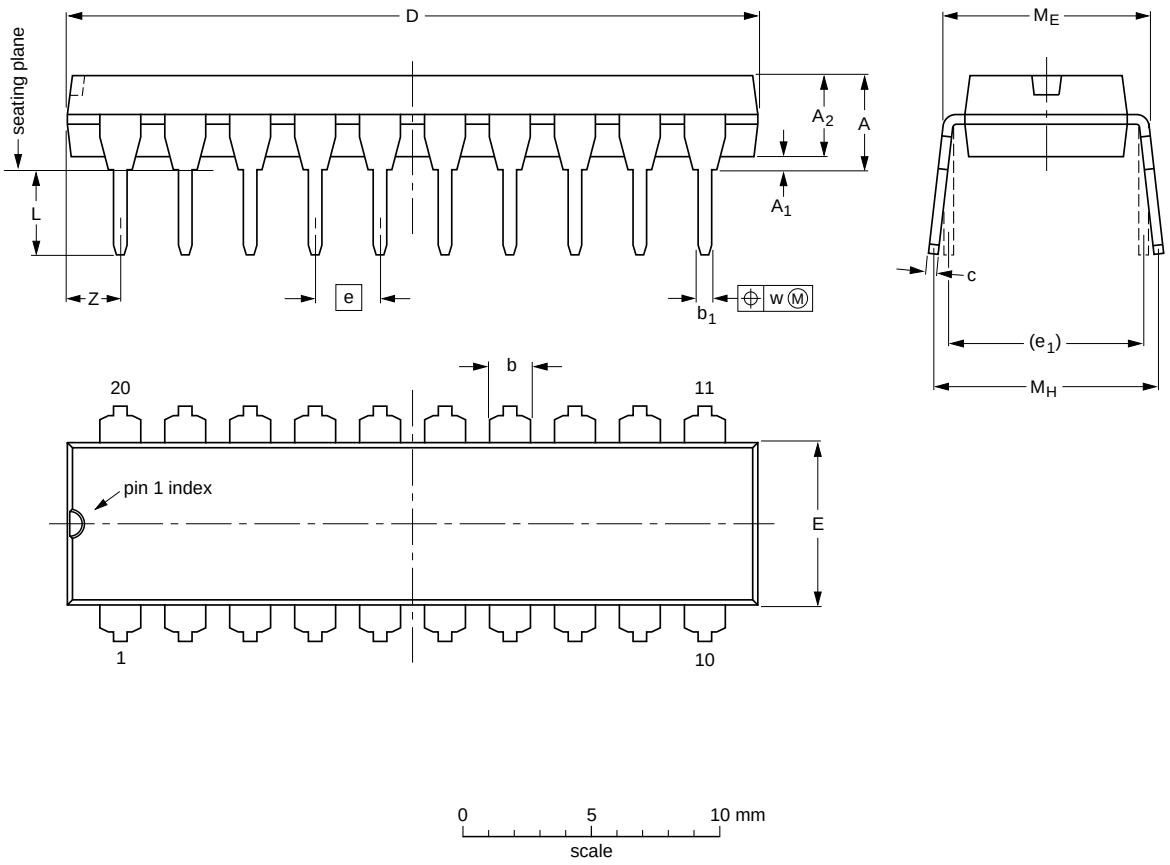
Fig 9. Test circuit for measuring switching times

Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

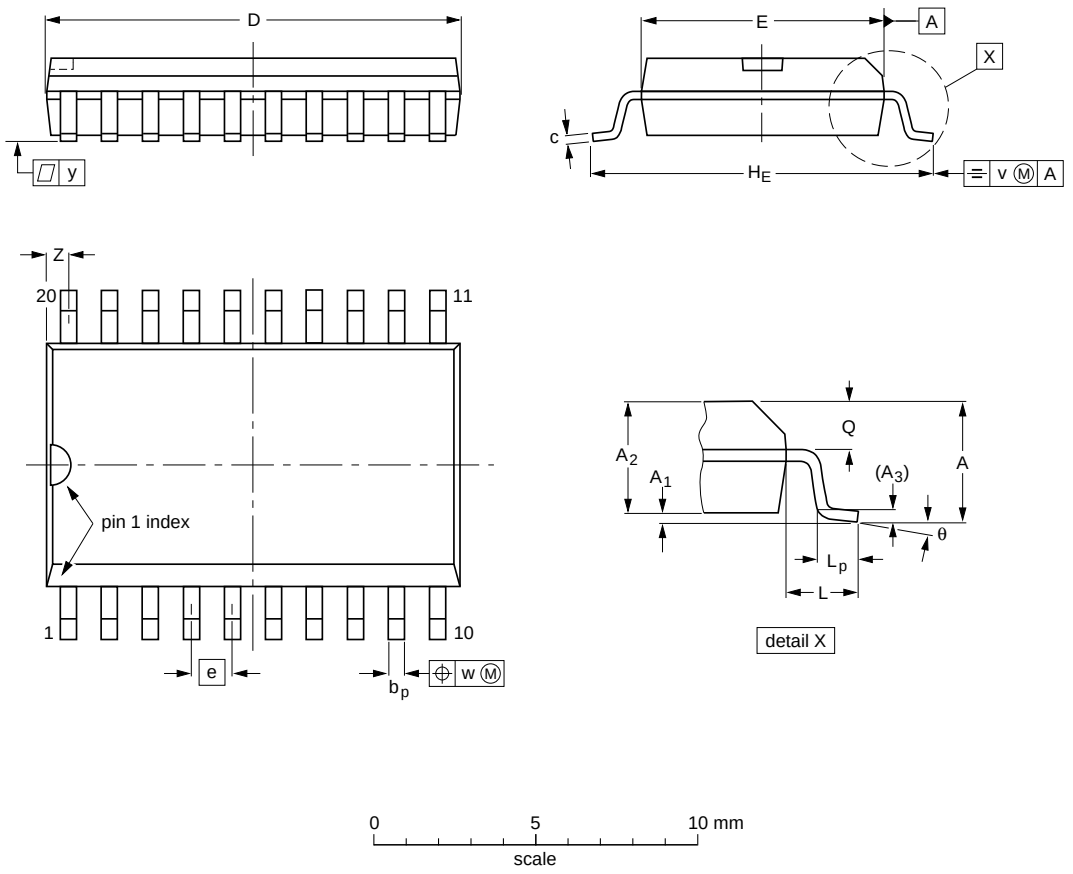
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT146-1		MS-001	SC-603			~~99-12-27~~ 03-02-13

Fig 10. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

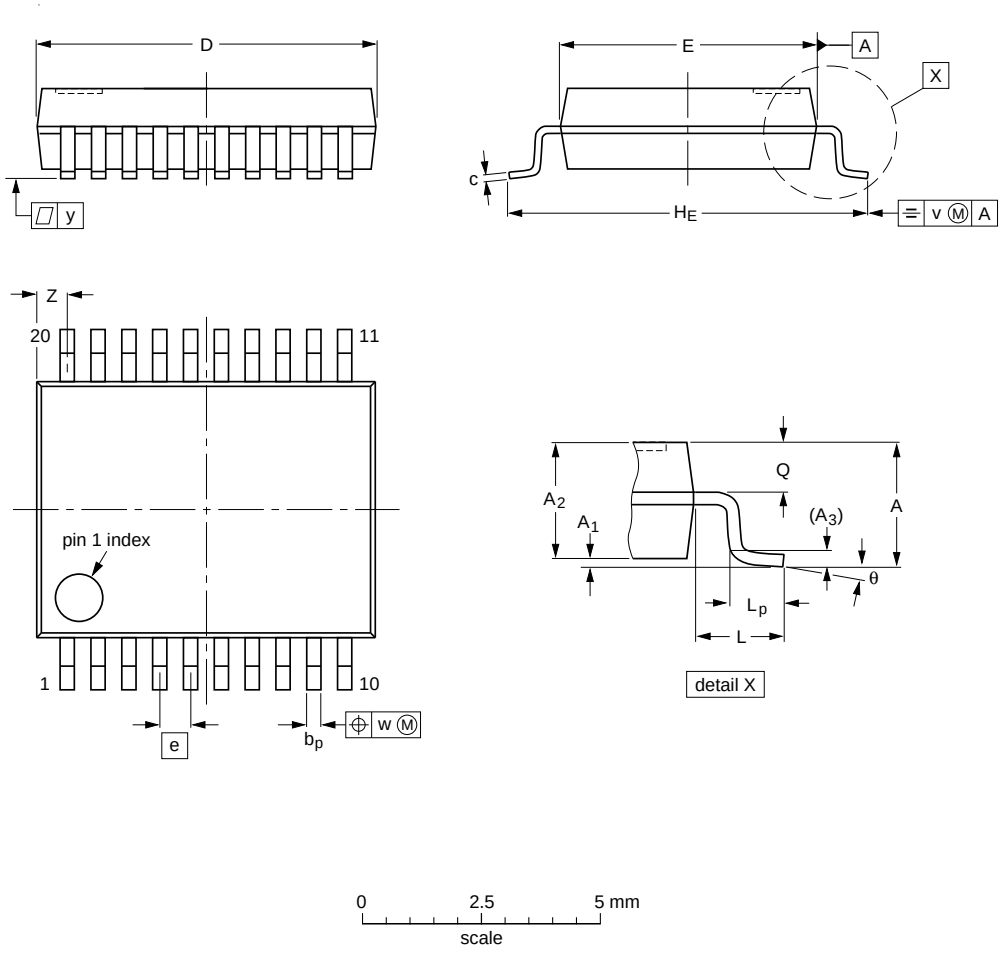
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

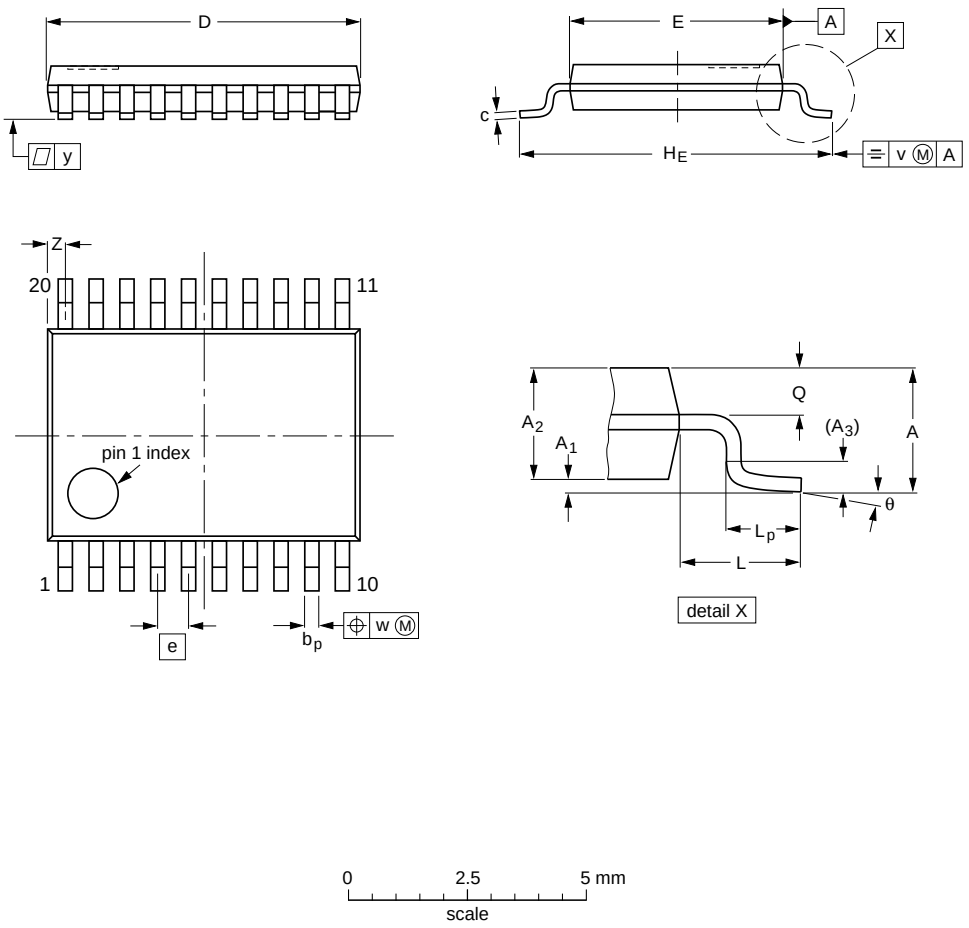
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT360-1 (TSSOP20)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT574A v.2	20121123	Product data sheet	-	74ABT574A v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74ABT574A v.1	19950522	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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