Rayson *Bluetooth® Module*

BC08 Class2 Stereo ROM Module BTM-640/645

Features

- The module is a Max.4dBm(Class2) module.
- Fully Qualified Bluetooth v3.0.
- Integrated Switched-Mode Regulator.
- Integrated Battery Charger.
- Embedded Kalimba DSP Co-Processor.
- Integrated 16-bit Stereo Audio CODEC 93dB SNR for DAC.
- CSR's latest CVC technology for narrowband and wideband voice connections including wind noise reduction.
- Wideband speech supported by HFP v1.6 Profile and mSBC codec.
- Multipoint HFP connection to 2 phones for voice.
- Multipoint A2DP connection enables a headset(A2DP) connection to 2 A2DP source device for music playback.
- Support Digital Audio Bus : PCM and I^2S.
- Support Host Interface: USB2.0 or UART.
- SBC, MP3, AAC, Faststream(BTM640), APTX(BTM645) decoder support.
- HSP v1.2/ HFP v1.6/ A2DP v1.2/ AVRCP v1.4
- Voice prompts (SPI Flash)
- RoHS compliant.
- Small outline. 13.4 x13.4 x2.7mm(8M SPI Flash)
  13.4 x13.4 x1.9mm(64K EEPROM)

Outline

Applications

- Stereo Wireless Headsets.
- Wired stereo headsets and headphones.
- Portable stereo speakers.

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General Electrical Specification

Absolute Maximum Ratings:		
Ratings	**Min.**	**Max.**
Storage Temperature	**-40 ℃**	**+85 ℃**
Supply Voltage (VCHG)	**-0.4V**	**5.75V**
Supply Voltage (VREG_ENABLE,VBAT_SENSE)	**-0.4V**	**4.2V**
Supply Voltage (LED[2:0])	**-0.4V**	**4.4V**
Supply Voltage (PIO_POWER)	**-0.4V**	**3.6V**
Recommended Operating Condition:		
Operating Condition		
Operating Temperature range	**-20 ℃**	**+75 ℃**
Supply Voltage (VBAT)	**2.7V**	**4.25V**
Supply Voltage (VCHG)	**4.75V / 3.10 V**	**5.25V**
Supply Voltage (VREG_ENABLE,VBAT_SENSE)	**0V**	**4.2V**
Supply Voltage (LED[2:0])	**1.10V**	**4.25V**
Supply Voltage (PIO_POWER)*	**1.7V**	**3.6V**

1.8V Switch-mode Regulator

1.8V Switch-mode Regulator	**Min**	**Typ**	**Max**	**Unit**
Input voltage (VBAT)	2.70	3.70	4.25	V
Output voltage (1V8_SMPS)	1.70	1.80	1.90	V
Normal Operation				
Transient settling time	-	30	-	µs
Load current	-	-	185	mA
Current available for external use, stereo audio with 16Ω load[(a)]	-	-	25	mA
Peak conversion efficiency	-	90	-	%
Switching frequency	3.63	4.00	4.00	MHz
Low-power Mode, Automatically Entered in Deep Sleep				
Transient settling time	-	200	-	µs
Load current	0.005	-	5	mA
Current available for external use	-	-	5	mA
Peak conversion efficiency	-	85	-	%
Switching frequency	100	-	200	kHz

(a) More current available for audio loads above 16Ω.

Regulator Enable

VREG_ENABLE, Switching Threshold	Min	Typ	Max	Unit
Rising threshold	1.0	-	-	V

Battery Charger

Battery Charger	Min	Typ	Max	Unit
Input voltage, VCHG[(a)]	4.75 / 3.10	5.00	5.25	V

(a) Reduced specification from 3.1 to 4.75. Full specification > 4.75V.

Trickle Charge Mode		Min	Typ	Max	Unit
Charge current $I_{trickle}$, as percentage of fast charge current		8	10	12	%
V_{fast} rising threshold		-	2.9	-	V
V_{fast} rising threshold trim step size		-	0.1	-	V
V_{fast} falling threshold		-	2.8	-	V
Fast Charge Mode		**Min**	**Typ**	**Max**	**Unit**
Charge current during constant Current mode, I_{fast}	Max, headroom > 0.55V	194	200	206	mA
	Min, headroom > 0.55V		10		mA
Reduced headroom charge current, As a percentage of I_{fast}	Mid, headroom=0.15V	50	-	100	%
I-CTRL charge current step size		-	10	-	mA
V_{float} threshold, calibrated		4.16	4.20	4.24	V
Standby Mode		**Min**	**Typ**	**Max**	**Unit**
Voltage hysteresis on VBAT, V_{hyst}		100	-	150	mV
Error Charge Mode		**Min**	**Typ**	**Max**	**Unit**
Headroom[(a)] error rising threshold		30	-	50	mV
Headroom[(a)] error threshold hysteresis		20	-	30	mV

(a) Headroom=VCHG-VBAT

External Charge Mode	Min	Typ	Max	Unit
Fast charge current, I_{fast}	200	-	500	mA
Control current into CHG_EXT	0	-	20	mA
Voltage on CHG_EXT	0		5.75	V
External pass device h_{fe}	-	50	-	-
Sense voltage, between VBAT_SENSE and VBAT at maximum current	195	200	205	mV

(a) In the external mode, the battery charger meets all the previous charger electrical characteristics and the additional or superseded electrical characteristics are listed in this table.

Stereo Codec: Analogue to Digital Converter

Analogue to Digital Converter					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**

Resolution	-		-	-	16	Bits
Input Sample Rate, Fsample	-		8	-	48	kHz
SNR	fin = 1kHz B/W = 20Hz→Fsample/2 (20kHz max) A-Weighted THD+N < 1% 1.6Vpk-pk input	F_{sample}				
		8kHz	-	92	-	dB
		16kHz	-	89	-	dB
		32kHz	-	88	-	dB
		44.1kHz	-	88	-	dB
		48kHz	-	88	-	dB
THD+N	fin = 1kHz B/W = 20Hz→Fsample/2 (20kHz max) 1.6Vpk-pk input	F_{sample}				
		8kHz	-	0.0036	-	%
		48kHz	-	0.0052	-	%
Digital gain	Digital gain resolution = 1/32		-24	-	21.5	dB
Analogue gain	Pre-amplifier setting = 0dB, 9dB, 21dB or30dB Analogue setting = -3dB to 12dB in 3dB steps		-3	-	42	dB
Stereo separation (crosstalk)			-	-86	-	dB

Stereo Codec: Digital to Analogue Converter

Digital to Analogue Converter							
Parameter	**Conditions**			**Min**	**Typ**	**Max**	**Unit**
Resolution	-			-	-	16	Bits
Output Sample Rate, Fsample	-			8	-	96	kHz
SNR	fin = 1kHz B/W = 20Hz→20kHz A-Weighted THD+N < 0.1% 0dBFS input	**Fsample**	**Load**				
		48kHz	100kΩ	-	92	-	dB
		48kHz	32Ω	-	93	-	dB
		48kHz	16Ω	-	93	-	dB
THD+N	fin = 1kHz B/W = 20Hz→20kHz 0dBFS input	**Fsample**	**Load**				
		8kHz	100kΩ	-	0.0019	-	%
		8kHz	32Ω	-	0.0024	-	%
		8kHz	16Ω	-	0.0032	-	%
		48kHz	100kΩ	-	0.0026	-	%
		48kHz	32Ω	-	0.0036	-	%
		48kHz	16Ω	-	0.0052	-	%
Digital Gain	Digital Gain Resolution = 1/32			-24	-	21.5	dB

Analogue Gain	Analogue Gain Resolution = 3dB	-21	-	0	dB
Stereo separation (crosstalk)		-	-88	-	dB

Digital

Digital Terminals	Min	Typ	Max	Unit
Input Voltage				
V_{IL} input logic level low	-0.4	-	0.4	V
V_{IH} input logic level high	0.7xPIO_POWER	-	PIO_POWER+0.4	V
Tr/Tf	-	-	25	ns
Output Voltage				
V_{OL} output logic level low, I_{OL} = 4.0mA	-	-	0.4	V
V_{IH} output logic level high, I_{OH} = -0.4mA	0.75xPIO_POWER	-	-	V
Tr/Tf	-	-	5	ns
Input and Tristate Currents				
Strong pull-up	-150	-40	-10	uA
Strong pull-down	10	40	150	uA
Weak pull-up	-5	-1.0	-0.33	uA
Weak pull-down	0.33	1.0	5.0	uA
C_I input Capacitance	1.0		5.0	pF

LED Driver Pads

LED Driver Pads		Min	Typ	Max	Unit
Current, I_{PAD}	High impedance state	-	-	5	µA
	Current sink state	-	-	10	mA
LED pad voltage, V_{PAD}	I_{PAD} = 10mA	-	-	0.55	V
LED pad resistance	V_{PAD} < 0.5V	-	-	40	Ω
V_{OL} output logic level low[(a)]		-	0	-	V
V_{OH} output logic level high[(a)]		-	0.8	-	V
V_{IL} input logic level low		-	0	-	V
V_{IH} input logic level high		-	0.8	-	V

(a) LED output port is open-drain and requires a pull-up

Auxiliary ADC

Auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	10	Bits
Input voltage range(a)		0	-	1.35	V
Accuracy	INL	-1	-	1	LSB
(Guaranteed monotonic)	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain error		-0.8	-	0.8	%

Input bandwidth	-	100	-	kHz
Conversion time	1.38	1.69	2.75	µs
Sample rate(b)	-	-	700	Samples/s

(a) LSB size = VDD_AUX/1023

(b) The auxiliary ADC is accessed through a VM function. The sample rate given is achieved as part of this function.

Auxiliary DAC

Auxiliary DAC	Min	Typ	Max	Unit
Resolution	-	-	10	Bits
Supply voltage, VDD_DAC	1.30	1.35	1.40	V
Output voltage range	0	-	1.35	V
Full-scale output voltage	1.30	1.35	1.40	V
LSB size	0	1.32	2.64	mV
Offset	-1.32	0	1.32	mV
Integral non-linearity	-1	0	1	LSB
Settling time(a)	-	-	250	ns

(a) The settling time does not include any capacitive load

Power Consumption

DUT Role	Connection		Packet Type	Packet Size	Average Current	Unit
Slave	SCO		HV3	30	TBD	mA
Slave	eSCO		EV3	30	TBD	mA
Slave	eSCO		2EV3	60	TBD	mA
Slave	eSCO		2EV3	30	TBD	mA
Slave	SCO	2-mic CVC	HV3	30	TBD	mA
Slave	eSCO	2-mic CVC	2EV3	60	TBD	mA
Slave	eSCO	2-mic CVC	2EV3	30	TBD	mA
Slave	Stereo high quality: ■ SBC ■ 350kbps ■ No sniff		TBD	TBD	TBD	mA
Slave	Stereo high quality: ■ SBC ■ 350kbps ■ Sniff		TBD	TBD	TBD	mA

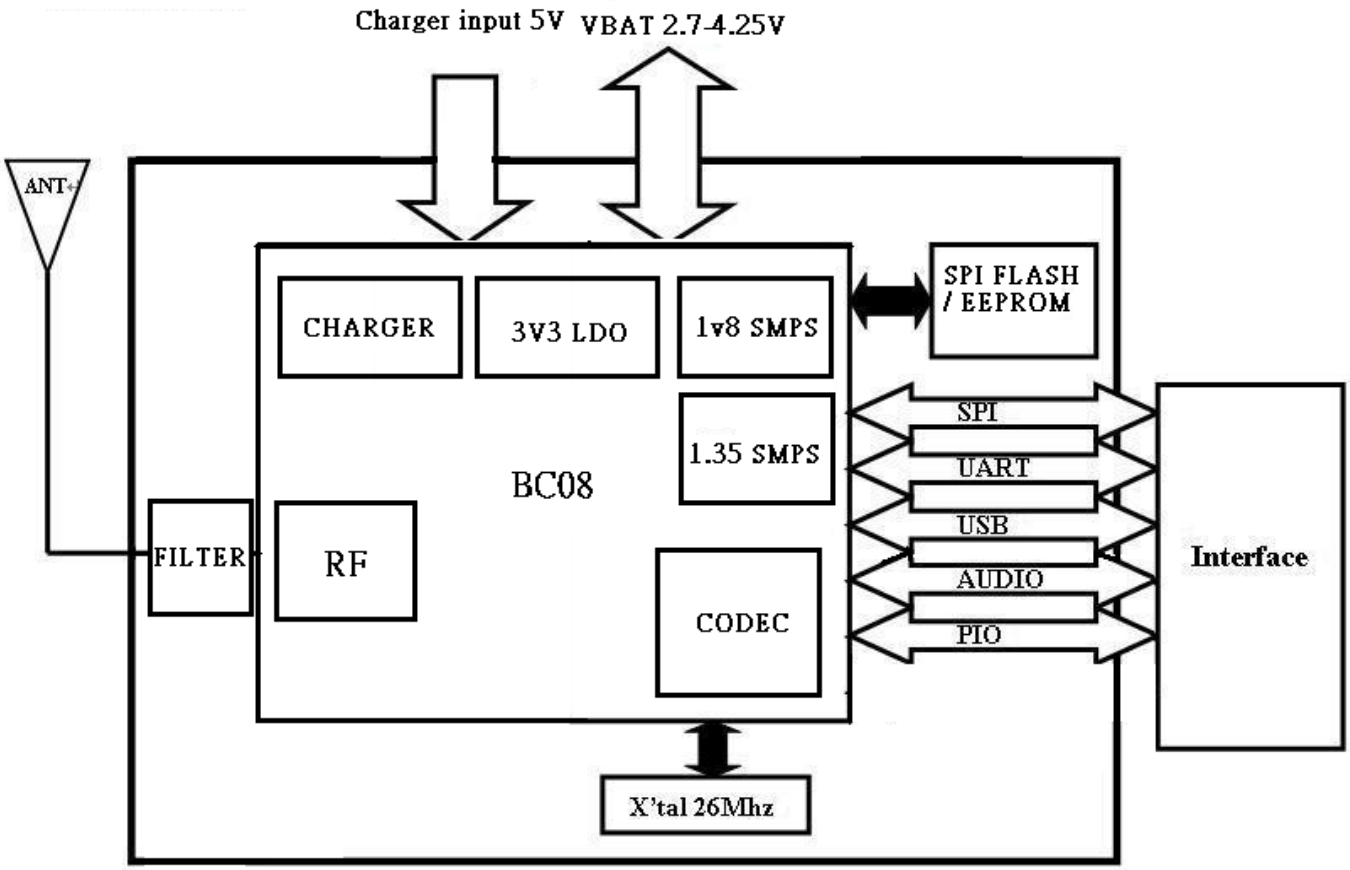
Slave	Stereo high quality: ■ MP3 ■ 128kbps ■ No sniff		TBD	TBD	TBD	mA
Slave	Stereo high quality: ■ MP3 ■ 128kbps ■ Sniff		TBD	TBD	TBD	mA
Slave	ACL	Sniff = 100ms	-	-	TBD	mA
Slave	ACL	Sniff = 500ms	-	-	TBD	mA
Slave	ACL	Sniff = 1280ms	-	-	TBD	mA
Master	SCO		HV3	30	TBD	mA
Master	eSCO		EV3	30	TBD	mA
Master	eSCO		2EV3	60	TBD	mA
Master	eSCO		2EV3	30	TBD	mA
Master	SCO	2-mic CVC	HV3	30	TBD	mA
Master	eSCO	2-mic CVC	2EV3	60	TBD	mA
Master	eSCO	2-mic CVC	2EV3	30	TBD	mA
Master	ACL	Sniff = 100ms	-	-	TBD	mA
Master	ACL	Sniff = 500ms	-	-	TBD	mA
Master	ACL	Sniff = 1280ms	-	-	TBD	mA

Note:

Current consumption values are taken with:

- VBAT pin = 3.7V
- RF TX power set to 0dBm
- No RF retransmissions in case of eSCO
- Microphones and speakers disconnected, with internal microphone bias circuit set to minimum current level
- Audio gateway transmits silence when SCO/eSCO channel is open
- LEDs disconnected

Block Diagram



RF Specification: Temperature=+20℃

Transmitter

	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power	-	TBD	-	-6 to +4	dBm
RF power control range	-	TBD	-	≥16	dB
RF power range control resolution	-	TBD	-	-	dB
20dB bandwidth for modulated carrier	-	TBD	-	≤1000	kHz
Adjacent channel transmit power F = F0 ± 2MHz	-	TBD	-	≤-20	dBm
Adjacent channel transmit power F = F0 ± 3MHz	-	TBD	-	≤-40	dBm
Adjacent channel transmit power F = F0 ± > 3MHz	-	TBD	-	≤-40	dBm
Δf1avg Maximum Modulation	-	TBD	-	140<f1avg<175	kHz

Δf2max Minimum Modulation	**-**	**TBD**	**-**	**115**	**kHz**
Δf1avg/Δf2avg	**-**	**TBD**	**-**	**≥0.80**	
Initial carrier frequency tolerance	**-**	**TBD**	**-**	**±75**	**kHz**
Drift Rate	**-**	**TBD**	**-**	**≤20**	**kHz/50μ**
Drift (single slot packet)	**-**	**TBD**	**-**	**≤25**	**kHz**
Drift (five slot packet)	**-**	**TBD**	**-**	**≤40**	**kHz**
2nd Harmonic Content	**-**	**TBD**	**-**	**≤-30**	**dBm**
3rd Harmonic Content	**-**	**TBD**	**-**	**≤-30**	**dBm**

Receiver

	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	**2.402**	**-**	**TBD**	**-**	**≤-70**	**dBm**
	2.441	**-**	**TBD**	**-**		
	2.480	**-**	**TBD**	**-**		
Maximum received signal at 0.1% BER		**-**	**TBD**		**≥-20**	**dBm**
C/I co-channel		**-**	**TBD**	**-**	**≤11**	**dB**
Adjacent channel selectivity C/I F = F0 + 1MHz		**-**	**TBD**	**-**	**≤0**	**dB**
Adjacent channel selectivity C/I F = F0 - 1MHz		**-**	**TBD**	**-**	**≤0**	**dB**
Adjacent channel selectivity C/I F = F0 + 2MHz		**-**	**TBD**	**-**	**≤-20**	**dB**
Adjacent channel selectivity C/I F = F0 - 2MHz		**-**	**TBD**	**-**	**≤-30**	**dB**
Adjacent channel selectivity C/I F = F0 - 3MHz		**-**	**TBD**	**-**	**≤-40**	**dB**
Adjacent channel selectivity C/I F = F0 + 5MHz		**-**	**TBD**	**-**	**≤-40**	**dB**
Adjacent channel selectivity C/I F = FImage		**-**	**TBD**	**-**	**≤-9**	**dB**
Maximum level of intermodulation interferers		**-**	**TBD**	**-**	**≥-39**	**dBm**
Spurious output level		**-**	**TBD**	**-**		**dBm/Hz**

BTM-640/645 Pin Functions

No.	Pin Name	Pin Type	Supply Domain	Pin Description
1	SPKR_R_N	Analogue	VDD_AUDIO_DRV (1V8_SMPS)	Speaker output negative, right
2	SPKR_R_P	Analogue	VDD_AUDIO_DRV (1V8_SMPS)	Speaker output positive, right
3	SPKR_L_N	Analogue	VDD_AUDIO_DRV (1V8_SMPS)	Speaker output negative, left
4	SPKR_L_P	Analogue	VDD_AUDIO_DRV (1V8_SMPS)	Speaker output positive, left
5	GND	GND		Common Ground
6.	RF_IO	Analogue		Connect to 50 ohm Antenna (RF Signal)
7.	GND	GND		Common Ground
8.	GND	GND		Common Ground
9.	GND	GND		Common Ground
10.	AIO0	Bi-directional	VDD_AUX(1.35V)	Analogue programmable input/output line
11.	PIO16	Bi-directional	PIO_POWER	Programmable input/output line
12.	PIO17	Bi-directional	PIO_POWER	Programmable input/output line
13.	RST#	Input with strong pull-up	PIO_POWER	Reset if low. Pull low for minimum 5ms to cause a reset
14	LED0	Open drain output	PIO_POWER	LED Driver
15	LED1	Open drain output	PIO_POWER	LED Driver
16.	PIO4	Bi-directional	PIO_POWER	Programmable input/output line Altemative functions: ■ SPI_CSB:chip select for SPI, active low ■ PCM1_SYNC: PCM1 synchronous data sync
17.	PIO2	Bi-directional	PIO_POWER	Programmable input/output line Altemative functions: ■ SPI_MOSI:SPI data input ■ PCM1_IN: PCM1 synchronous data input
18.	PIO5	Bi-directional	PIO_POWER	Programmable input/output line Altemative functions:

				■ SPI_CLK:SPI clock ■ PCM1_CLK: PCM1 synchronous data clock
19.	PIO3	Bi-directional	PIO_POWER	Programmable input/output line Altemative functions: ■ SPI_MISO:SPI data output ■ PCM1_OUT: PCM1 synchronous data output
20.	PIO_POWER	VDD		Positive supply for PIO
21.	VREG_ENABLE	Analogue		Regulator enable input
22.	SPI/PCM#	Input with weak pull-down	PIO_POWER	SPI/PCM# select input: ■ 0=PCM/PIO interface ■ 1=SPI
23.	VCHG	Charger input		Lithium ion/polymer battery charger input
24.	GND	GND		Common Ground
25.	CHG_EXT			External charger control. Otherwise leave unconnected.
26.	VBAT_SENSE			Battery charger sense input
27.	VBAT	Battery terminal +ve		Lithium ion/polymer battery positive terminal. Battery charger output and input to switch-mode regulator
28.	1V8_SMPS	VDD		1V8 Output
29.	PIO6	Bi-directional	PIO_POWER	Programmable input/output line
30.	PIO7	Bi-directional	PIO_POWER	Programmable input/output line
31.	PIO18	Bi-directional	PIO_POWER	Programmable input/output line
32.	PIO19	Bi-directional	PIO_POWER	Programmable input/output line
33.	PIO21	Bi-directional	PIO_POWER	Programmable input/output line
34.	PIO20	Bi-directional	PIO_POWER	Programmable input/output line
35.	PIO9	Bi-directional	PIO_POWER	Programmable input/output line
36.	GND	GND		Common Ground
37.	PIO0	Bi-directional	PIO_POWER	Programmable input/output line
38.	PIO1	Bi-directional	PIO_POWER	Programmable input/output line
39.	PIO8	Bi-directional	PIO_POWER	Programmable input/output line
40.	USB_DN	Bi-directional	3V3_USB	USB data minus
41.	USB_DP	Bi-directional	3V3_USB	USB data plus
42.	LED2	Open drain output	PIO_POWER	LED Driver
43	MIC_BIAS	Analogue	VBAT/3V3_USB	Microphone bias
44.	MIC_BN	Analogue	VDD_AUDIO(1.35V)	Microphone input negative,

				right
45.	**MIC_BP**	**Analogue**	**VDD_AUDIO(1.35V)**	**Microphone input positive, right**
46.	**MIC_AN**	**Analogue**	**VDD_AUDIO(1.35V)**	**Microphone input negative, left**
47.	**MIC_AP**	**Analogue**	**VDD_AUDIO(1.35V)**	**Microphone input positive, left**
48.	**GND**	**GND**		**Common Ground**

1. Serial Interface

1.1 USB Interface

BTM-640/650 has a full-speed (12Mbps) USB interface for communicating with other compatible digital devices. The USB interface on BTM-640/645 acts as a USB peripheral, responding to requests from a master host controller. BTM-640/645 contains internal USB termination resistors and requires no external resistor matching.

BTM-640/645 supports the Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification), supports USB standard charger detection and fully supports the USB Battery Charging Specification , available from http://www.usb.org. For more information on how to integrate the USB interface on BTM-640/645 see the Bluetooth and USB Design Considerations Application Note.

As well as describing USB basics and architecture, the application note describes:

- Power distribution for high and low bus-powered configurations
- Power distribution for self-powered configuration, which includes USB VBUS monitoring
- USB enumeration
- Electrical design guidelines for the power supply and data lines, as well as PCB tracks and the effects of ferrite beads
- USB suspend modes and Bluetooth low-power modes:
  - Global suspend
  - Selective suspend, includes remote wake
  - Wake on Bluetooth, includes permitted devices and set-up prior to selective suspend
  - Suspend mode current draw
  - PIO status in suspend mode
  - Resume, detach and wake PIOs
- Battery charging from USB, which describes dead battery provision, charge currents, charging in suspend modes and USB VBUS voltage consideration
- USB termination when interface is not in use
- Internal modules, certification and non-specification compliant operation

1.2 Programming and Debug Interface

BTM-640/645 provides a debug SPI interface for programming, configuring (PS Keys) and debugging the BTM640/645. Access to this interface is required in production. Ensure the 4 SPI signals and the SPI/PCM# line are brought out to either test points or a header. To use the SPI interface, the SPI/PCM# line requires the option of being pulled high externally.

1.2.1 Multi-slave Operation

Avoid connecting BTM-640/645 in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BTM640/645 is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, BTM-640/645 outputs 0 if the processor is running or 1 if it is stopped.

2. interfaces

2.1 Analogue I/O Ports, AIO

BTM-640/645 has 1 general-purpose analogue interface pin, AIO[0]. Typically, this connects to a thermistor for battery pack temperature measurements during charge control.

2.2 LED Drivers

BTM-640/645 includes a 3-pad synchronised PWM LED driver for driving RGB LEDs for producing a wide range of colours. All LEDs are controlled by firmware.

The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current-limiting resistor.

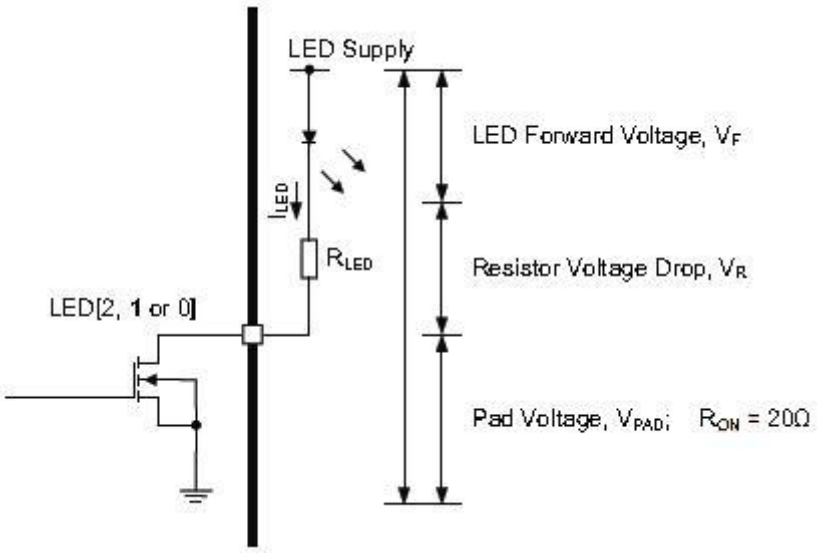


Figure 2.1: LED Equivalent Circuit

From Figure 2.1 it is possible to derive Equation 2.1 to calculate ILED. If a known value of current is required through the LED to give a specific luminous intensity, then the value of RLED is calculated.

$$I_{LED} = \frac{VDD - V_F}{R_{LED} + R_{ON}}$$

Equation 2.1: LED Current

For the LED pads to act as resistance, the external series resistor, RLED, needs to be such that the voltage drop across it, VR, keeps VPAD below 0.5V. Equation 2.2 also applies.

$$VDD = VF + VR + VPAD$$

Equation 2.2: LED PAD Voltage

Note:

The LED current adds to the overall current. Conservative LED selection extends battery life.

3. Power Control and Regulation

3.1 Voltage Regulator Enable

When using the integrated regulators the voltage regulator enable pin, VREG_ENABLE, enables the BTM-640/645 and the following regulators:

- 1.8V switch-mode regulator
- 1.35V switch-mode regulator
- Low-voltage VDD_DIG linear regulator
- Low-voltage VDD_AUX linear regulator

The VREG_ENABLE pin is active high.

BTM-640/645 boots-up when the voltage regulator enable pin is pulled high, enabling the regulators. The firmware

then latches the regulators on, it is then permitted to release the voltage regulator enable pin.

The status of the VREGENABLE pin is available to firmware through an internal connection. VREGENABLE also works as an input line.

3.2 Reset, RST#

BTM-640/645 is reset from several sources:

- RST# pin
- Power-on reset
- USB charger attach reset
- Software configured watchdog timer

The RST# pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. Rayson recommends applying RST# for a period >5ms.

At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are set to tristate.

3.3 Digital Pin States on Reset

Table 3.3.1 shows the pin states of BTM-640/645 on reset.

Pin Name / Group	I/O Type	Full Chip Reset
USB_DP	Digital bidirectional	N/A
USB_DN	Digital bidirectional	N/A
PIO[0]	Digital bidirectional	PUS
PIO[1]	Digital bidirectional	PUS
PIO[2]	Digital bidirectional	PDW
PIO[3]	Digital bidirectional	PDW
PIO[4]	Digital bidirectional	PDW
PIO[5]	Digital bidirectional	PDW
PIO[6]	Digital bidirectional	PDS
PIO[7]	Digital bidirectional	PDS
PIO[8]	Digital bidirectional	PUS
PIO[9]	Digital bidirectional	PDS
PIO[16]	Digital bidirectional	PUS
PIO[17]	Digital bidirectional	PDS
PIO[18]	Digital bidirectional	PDW
PIO[19]	Digital bidirectional	PDW
PIO[20]	Digital bidirectional	PDW
PIO[21]	Digital bidirectional	PDW

Table 3.3.1: Pin States on Reset

Note:

PUS = Strong pull-up

PDS = Strong pull-down

PUW = Weak pull-up

PDW = Weak pull-down

4. Battery Charger

4.1 Battery Charger hardware Operating Modes

The battery charger hardware is controlled by the VM. The battery charger has 5 modes:

- Disabled
- Trickle charge
- Fast charge
- Standby: fully charged or float charge
- Error: charging input voltage, VCHG, is too low

The battery charger operating mode is determined by the battery voltage and current.

The internal charger circuit can provide up to 200mA of charge current, for currents higher than this the BTM640/BTM645 can control an external pass transistor

4.2 External Mode

The external mode is for charging higher capacity batteries using an external pass device. The current is controlled by sinking a varying current into the CHG_EXT pin, and the current is determined by measuring the voltage drop across a resistor, Rsense, connected in series with the external pass device, see Figure 4.2.1. The voltage drop is determined by looking at the difference between the VBAT_SENSE and VBAT pins. The voltage drop across Rsense is typically 200mV. The value of the external series resistor determines the charger current. This current can be trimmed with a PS Key.

In Figure 4.2.1, R1 (220mΩ) and C1 (4.7µF) form a RC snubber that is required to maintain stability across all battery ESRs. The battery ESR must be <1.0Ω

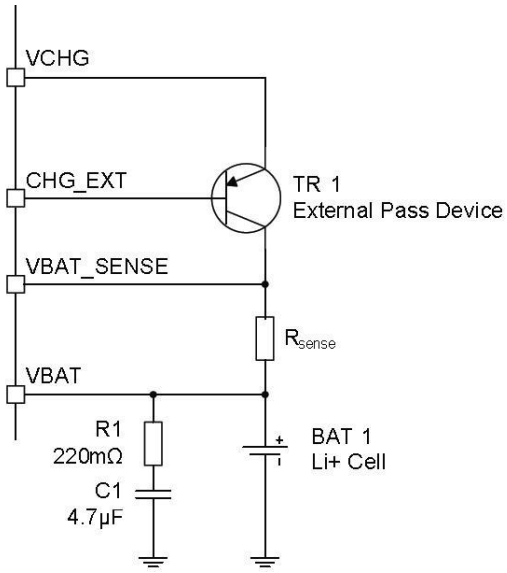


Figure 4.2.1: Battery Charger External Mode Typical Configuration

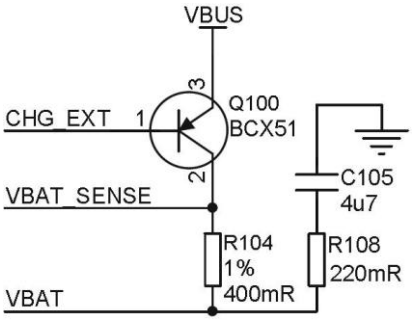


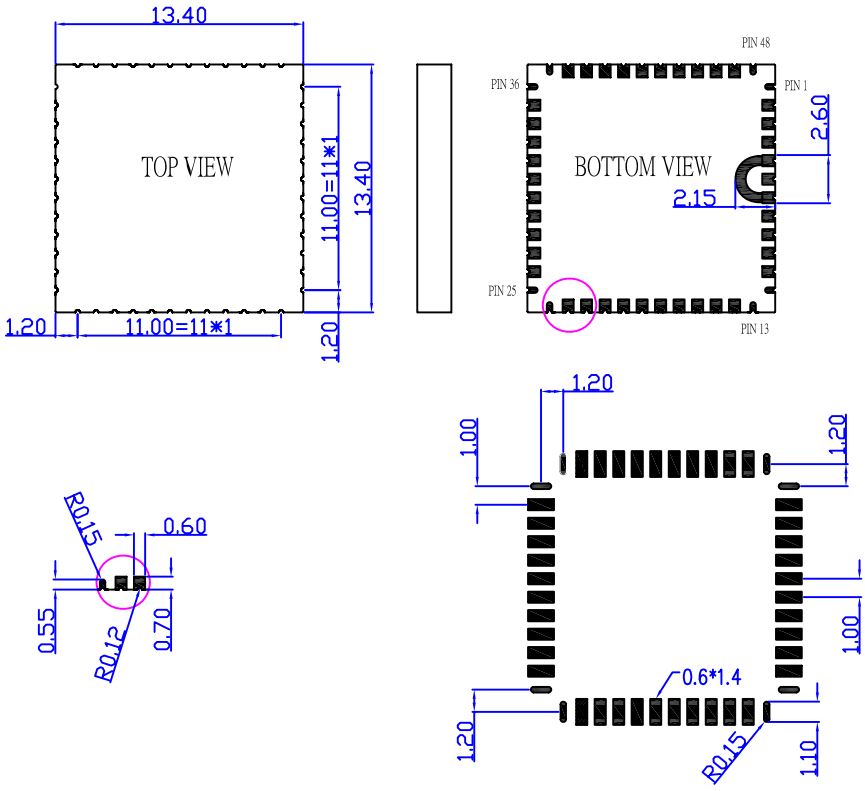
Figure 4.2.2: Optional Ancilliary Circuits

In Figure 4.2.2, Optional fast charge,400mΩ = 500m. Connect VBAT_SENSE to VBAT if not using this circuit.

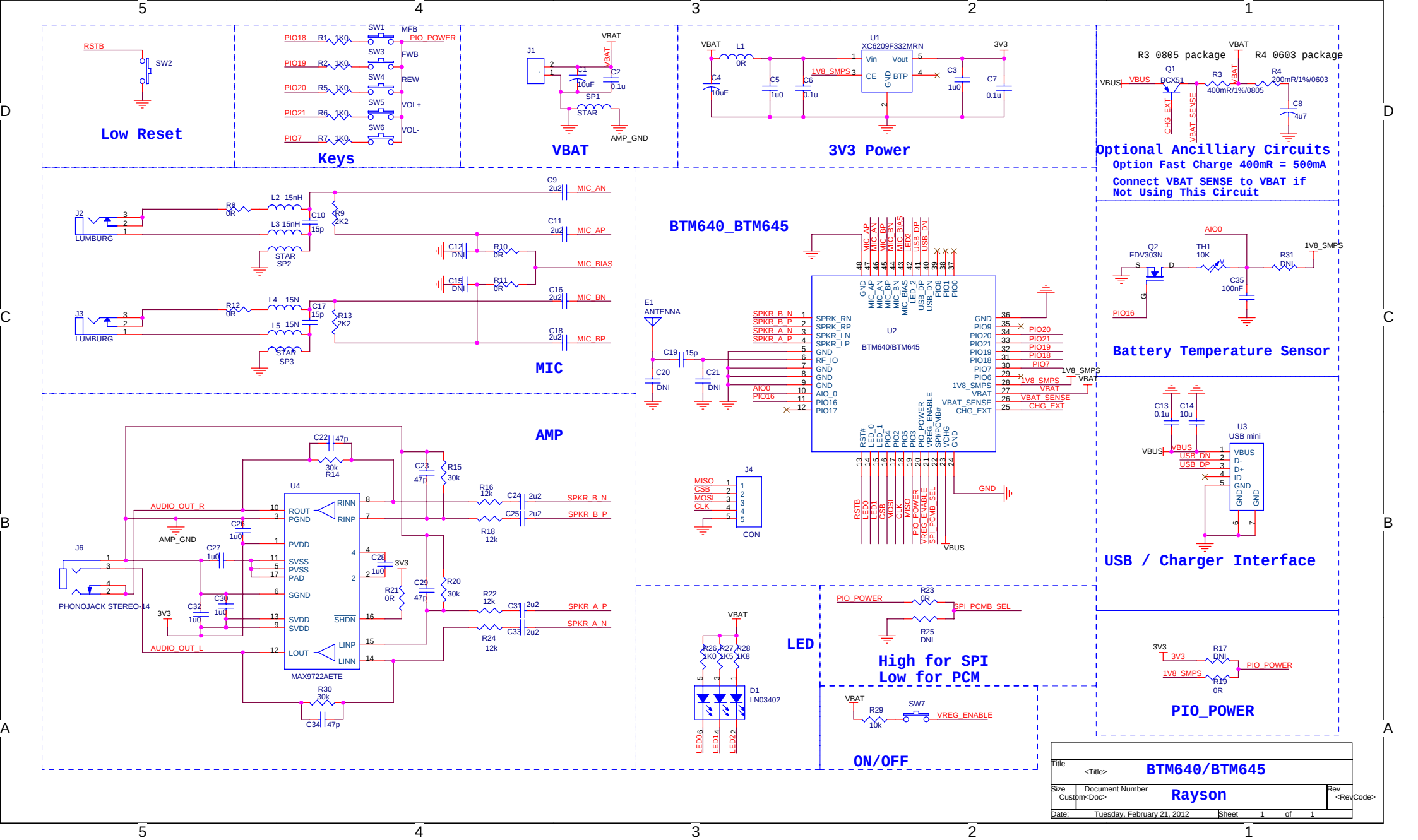
Dimension

Dimension

Unit: mm



PCB LAYOUT(TOP VIEW)


Low Reset
RSTB
SW2
Keys
PIO18
PIO19
PIO20
PIO21
PIO7
PIO_POWER
FWB
REW
VOL+
VOL-
MFB
VBAT
AMP_GND
3V3 Power
U1
XC6209F332MRN
1V8_SMPS
Optional Ancilliary Circuits
R3 0805 package
R4 0603 package
Option Fast Charge 400mR = 500mA
Connect VBAT_SENSE to VBAT if
Not Using This Circuit
MIC
LUMBURG
STAR
MIC_AN
MIC_AP
MIC_BIAS
MIC_BN
MIC_BP
BTM640_BTM645
BTM640/BTM645
ANTENNA
Battery Temperature Sensor
AIO0
PIO16
AMP
MAX9722AETE
AUDIO_OUT_R
AUDIO_OUT_L
PHONOJACK STEREO-14
SPKR_B_N
SPKR_B_P
SPKR_A_P
SPKR_A_N
USB / Charger Interface
USB mini
LED
D1
LN03402
High for SPI
Low for PCM
PIO_POWER
ON/OFF
VREG_ENABLE
Title
BTM640/BTM645
Rayson
Tuesday, February 21, 2012