aPR2060

Datasheet

40 ~ 80 sec recording voice IC

APLUS INTEGRATED CIRCUITS INC.

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■ FEATURES

- Operating Voltage Range: 3V ~ 6.5V
- Single Chip, High Quality Audio/Voice Recording & Playback Solution
  - ◆ No External ICs Required
  - ◆ Minimum External Components
- User Friendly, Easy to Use Operation
  - ◆ Programming & Development Systems Not Required
- 40 ~ 80 sec. Voice Recording Length
- Powerful 16-Bits Digital Audio Processor.
- Nonvolatile Flash Memory Technology
  - ◆ No Battery Backup Required
- External Reset pin.
- Powerful Power Management Unit
  - ◆ Very Low Standby Current: 1uA
  - ◆ Low Power-Down Current: 10uA
  - ◆ Supports Power-Down Mode for Power Saving
- Built-in Audio-Recording Microphone Amplifier
  - ◆ No External OPAMP or BJT Required
  - ◆ Easy to PCB layout
- Configurable analog interface
  - ◆ Differential-ended MIC pre-amp for Low Noise
  - ◆ High Quality Line Receiver
- High Quality Analog to Digital, DAC and PWM module
  - ◆ Resolution up to 16-bits
- Simple And Direct User Interface
- Averagely 1,2 or 4 voice messages record & playback
- Adjustable sample rates by external resistors

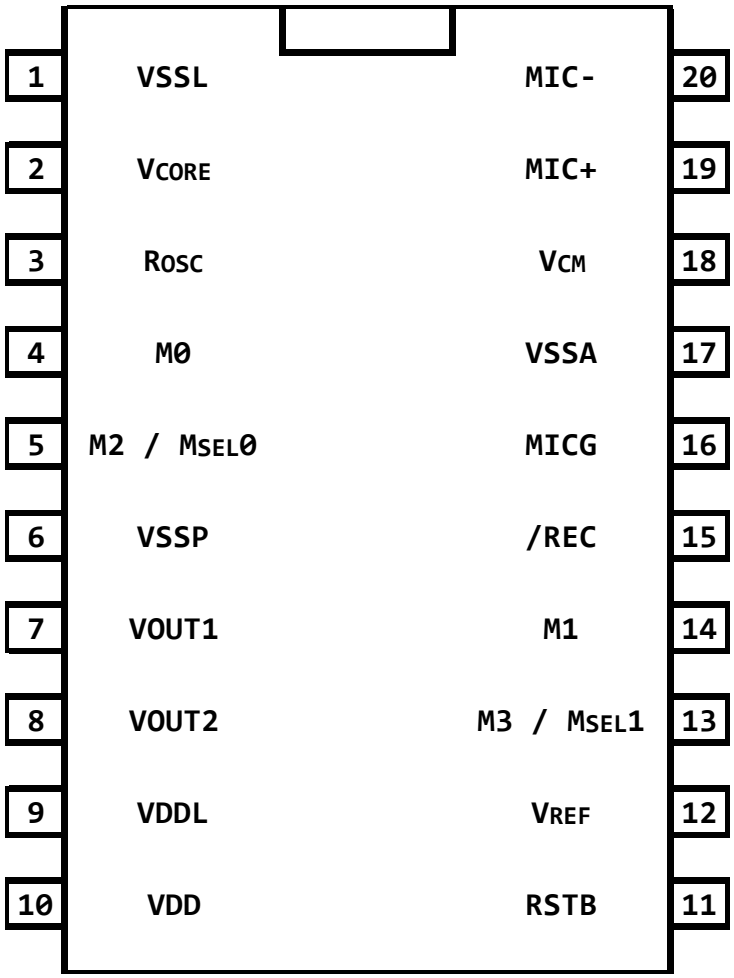
■ DESCRIPTION

Today's consumers demand the best in audio/voice. They want crystal-clear sound wherever they are in whatever format they want to use. APLUS delivers the technology to enhance a listener's audio/voice experience.

The aPR2060 is powerful audio processor along with high performance audio analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The aPR2060 are a fully integrated solution offering high performance and unparalleled integration with analog input, digital processing and analog output functionality. The aPR2060 incorporates all the functionality required to perform demanding audio/voice applications. High quality audio/voice systems with lower bill-of-material costs can be implemented with the aPR2060 because of its integrated analog data converters and full suite of quality-enhancing features such as sample-rate convertor.

The aPR2060 T2.2 is specially designed for simple key trigger, user can record and playback the message averagely for 1, 2 or 4 voice message(s) by switch, It is suitable in simple interface or need to limit the length of single message, e.g. toys, leave messages system, answering machine etc. Meanwhile, this mode provides the power-management system. Users can let the chip enter power-down mode when unused. It can effectively reduce electric current consuming to 10uA and increase the using time in any projects powered by batteries.

■ PIN CONFIGURATION

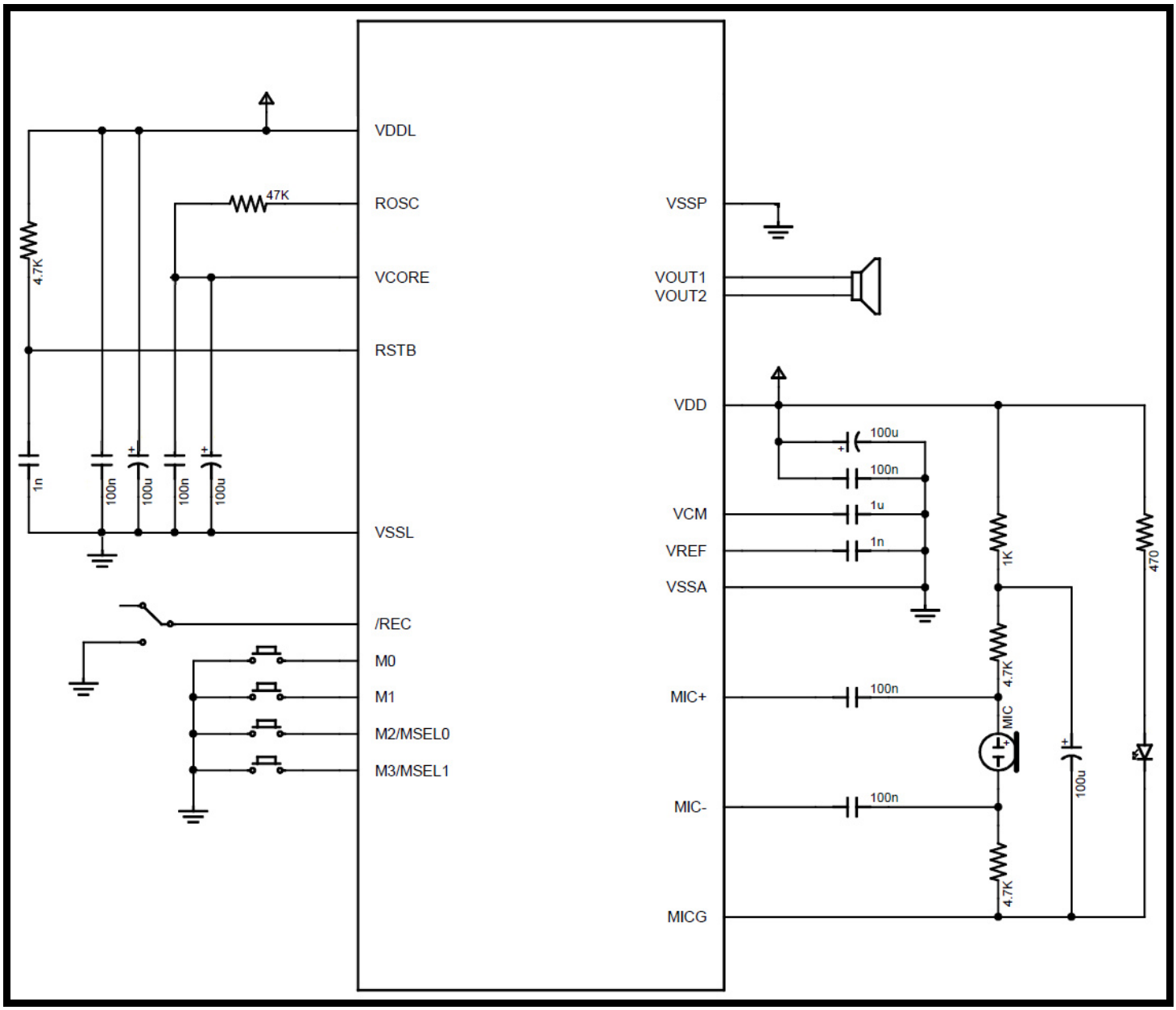


DIP / SOP 300mil Package

■ PIN DESCRIPTION

Pin Names	Pin No	TYPE	Description
VDDP VDD	9 10		Positive power supply.
VSSL VSSP VSSA	1 6 17		Power ground.
V_{CORE}	2		Positive power supply for core.
V_{REF}	12		Reference voltage.
V_{CM}	18		Common mode voltage.
Rosc	3	INPUT	Oscillator resistor input.
RSTB	11	INPUT	Reset. (Low active)
MIC+ MIC-	19 20	INPUT	Microphone differential input.
MICG	16	OUTPUT	Microphone ground.
VOUT1	7	OUTPUT	PWM output to drive speaker directly. DAC option.
VOUT2	8	OUTPUT	PWM output to drive speaker directly. DAC output.
/REC	15	INPUT	Record Mode. (Low active)
M0	4	INPUT	Message-0.
M1	14	INPUT	Message-1.
M2 / $M_{SEL}0$	5	INPUT	Message-6, Message select 0.
M3 / $M_{SEL}1$	13	INPUT	Message-7, Message select 1.

■ TYPICAL APPLICATION



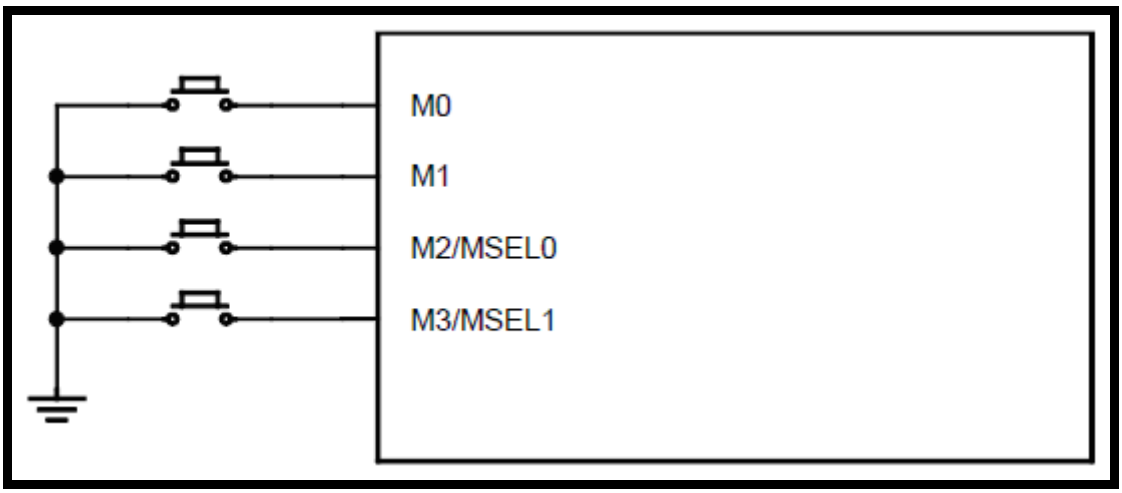
■ MESSAGE MODE

In fixed 1/ 2/ 4 message mode, user can divide the memory averagely for 1, 2 or 4 message(s). The message mode will be applied after chip reset by the MSEL0 and MSEL1 pin.

Please note the message should be recorded and played in same message mode, we CAN NOT guarantee the message is complete after message mode changed. For example, user recorded 4 messages in the 4-message mode, those messages can be played in 4-message mode only. If user changed to 1 or 2 message mode, system will discard those messages.

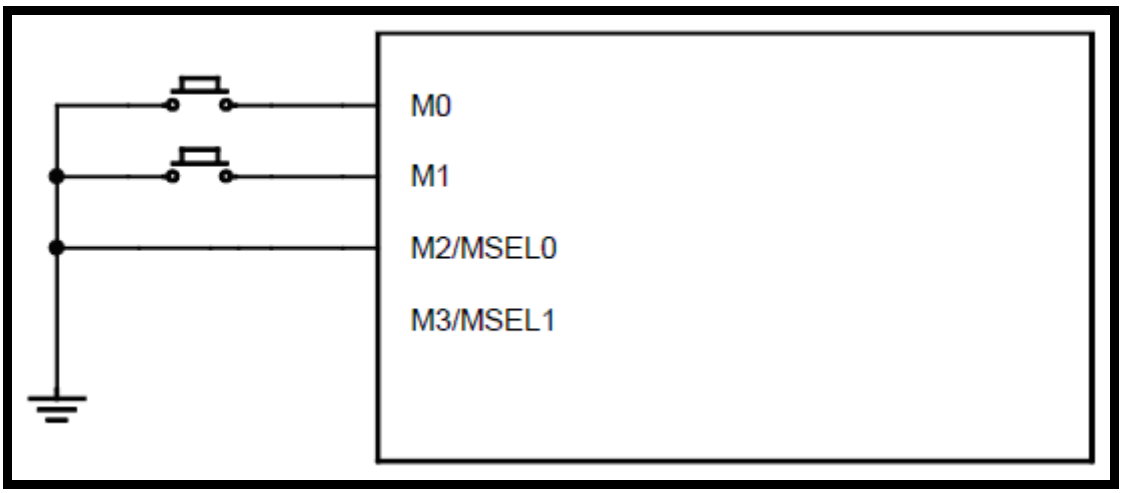
- 4-Message Mode

  The memory will be divided to 4 messages averagely when both MSEL0 and MSEL1 pin float after chip reset.



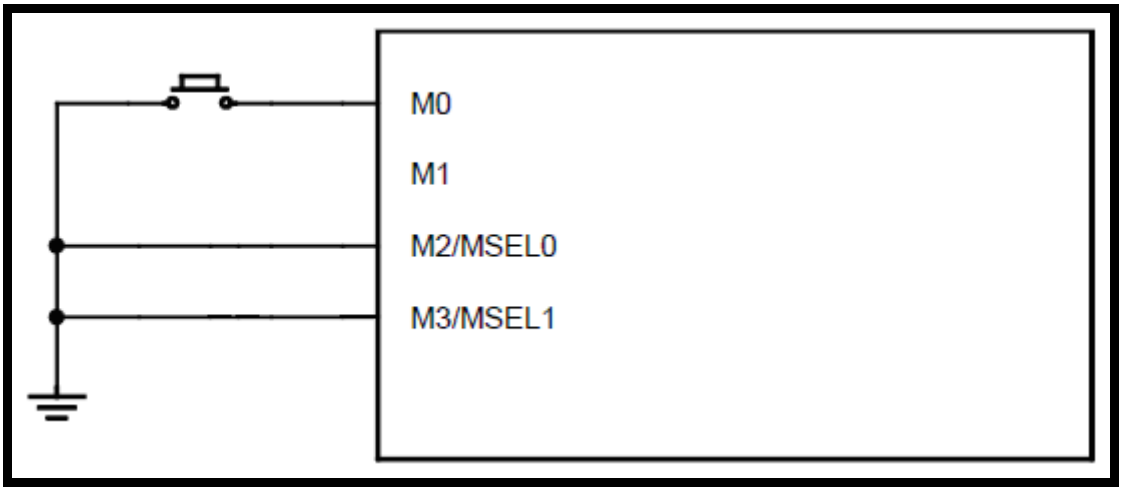
- 2-Message Mode

  The memory will be divided to 2 messages averagely when MSEL1 pin connected to VSS and MSEL0 pin float after chip reset.



- 1-Message Mode

  The memory will be for 1 message when both MSEL0 and MSEL1 pin connected to VSS after chip reset.



■ RECORD MESSAGE

During the /REC pin drove to V_{IL}, chip in the record mode.

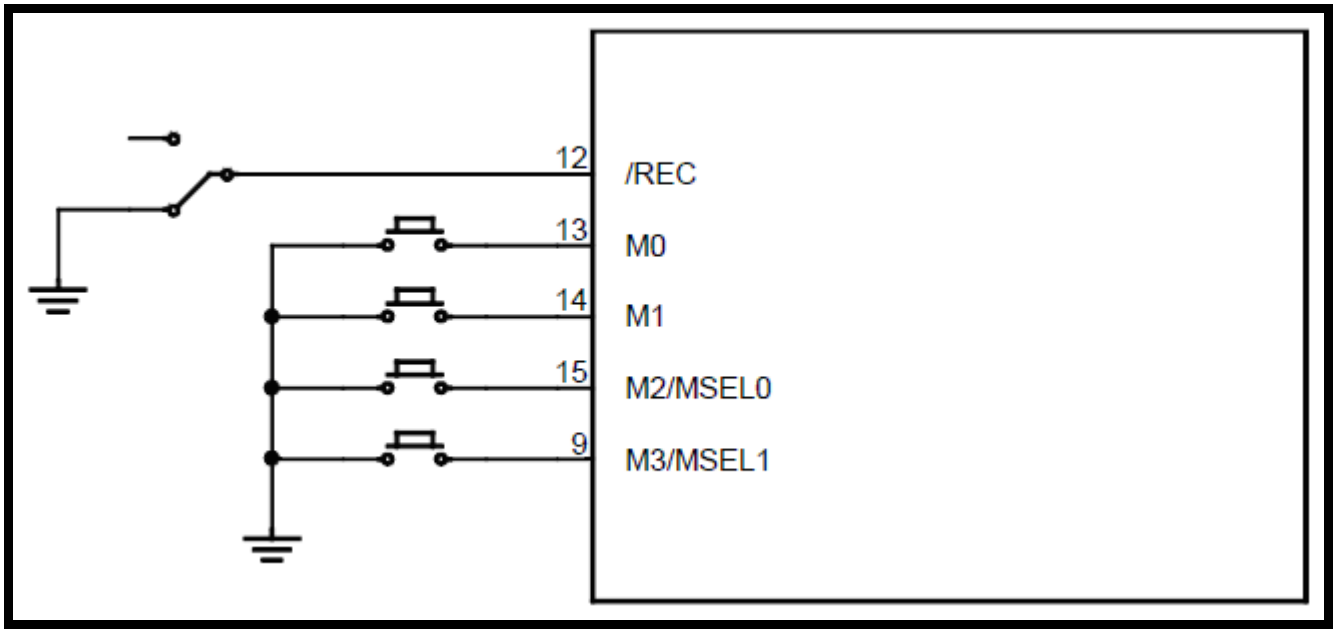
When the message pin (M0, M1, M2 or M3) drove to V_{IL} in record mode, the chip will playback “beep” tone and message record starting.

The message record will continue until message pin released or full of this message, and the chip will play “beep” tone to indicate the message record finished.

If the message already exist and user record again, the old one’s message will be replaced.

The following fig. showed a typical record circuit for 4-message mode. We connected a slide-switch between /REC pin and VSS, and connected 4 tact-switches between M0 ~ M3 pin and VSS. When the slide-switch fixed in VSS side and any tact-switch will be pressed, chip will start message record.

Note: After reset, /REC and M0 to M3 pin will be pull-up to VDD by internal resistor.



■ PLAYBACK MESSAGE

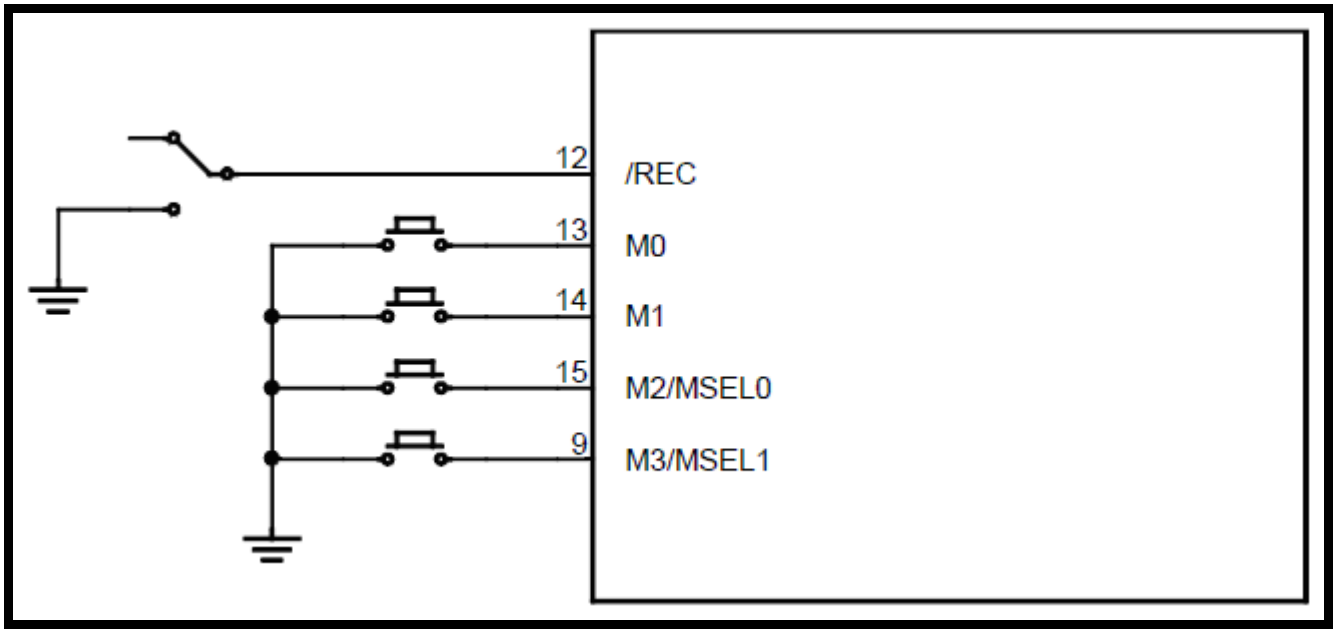
During the /REC pin drove to V_{IH}, chip in the playback mode.

When the message pin (M0, M1, M2 or M3) drove from V_{IH} to V_{IL} in playback mode, the message playback starting.

The message playback will continue until message pin drove from V_{IH} to V_{IL} again or end of this message.

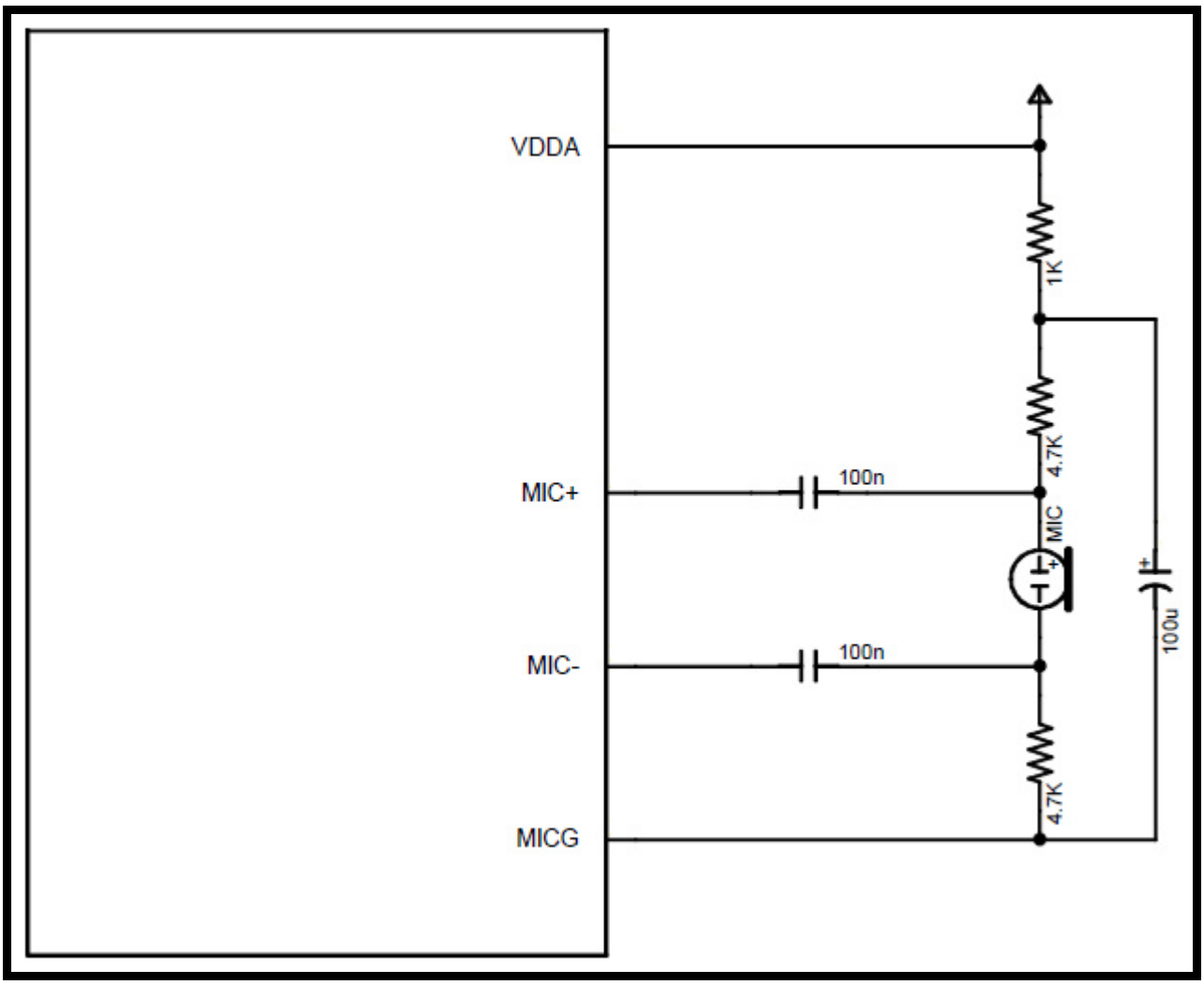
The following fig. showed a typical playback circuit for 4-message mode. We connected a slide-switch between /REC and VSS, and connected 4 tact-switches between M0 ~ M3 and VSS. When the slide-switch fixed in float side and any tact-switch will be pressed, chip will start message playback and until the user pressed the tact-switch again or end of message.

Note: After reset, /REC and M0 to M3 pin will be pull-up to VDD by internal resistor.

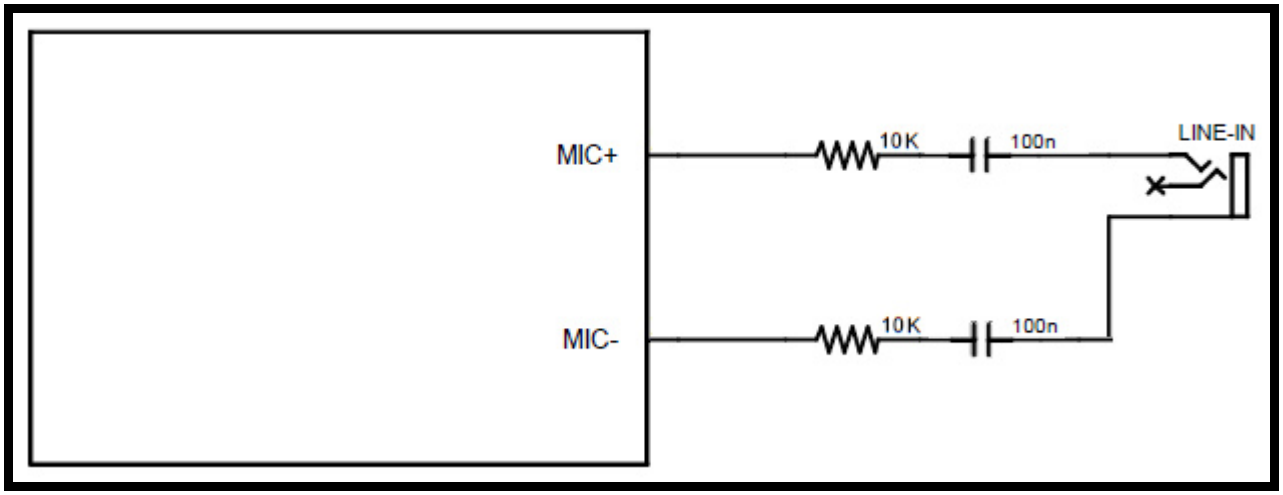


■ VOICE INPUT

The aPR2060 supported single channel voice input by microphone or line-in. The following fig. showed circuit for different input methods: microphone, line-in and mixture of both.

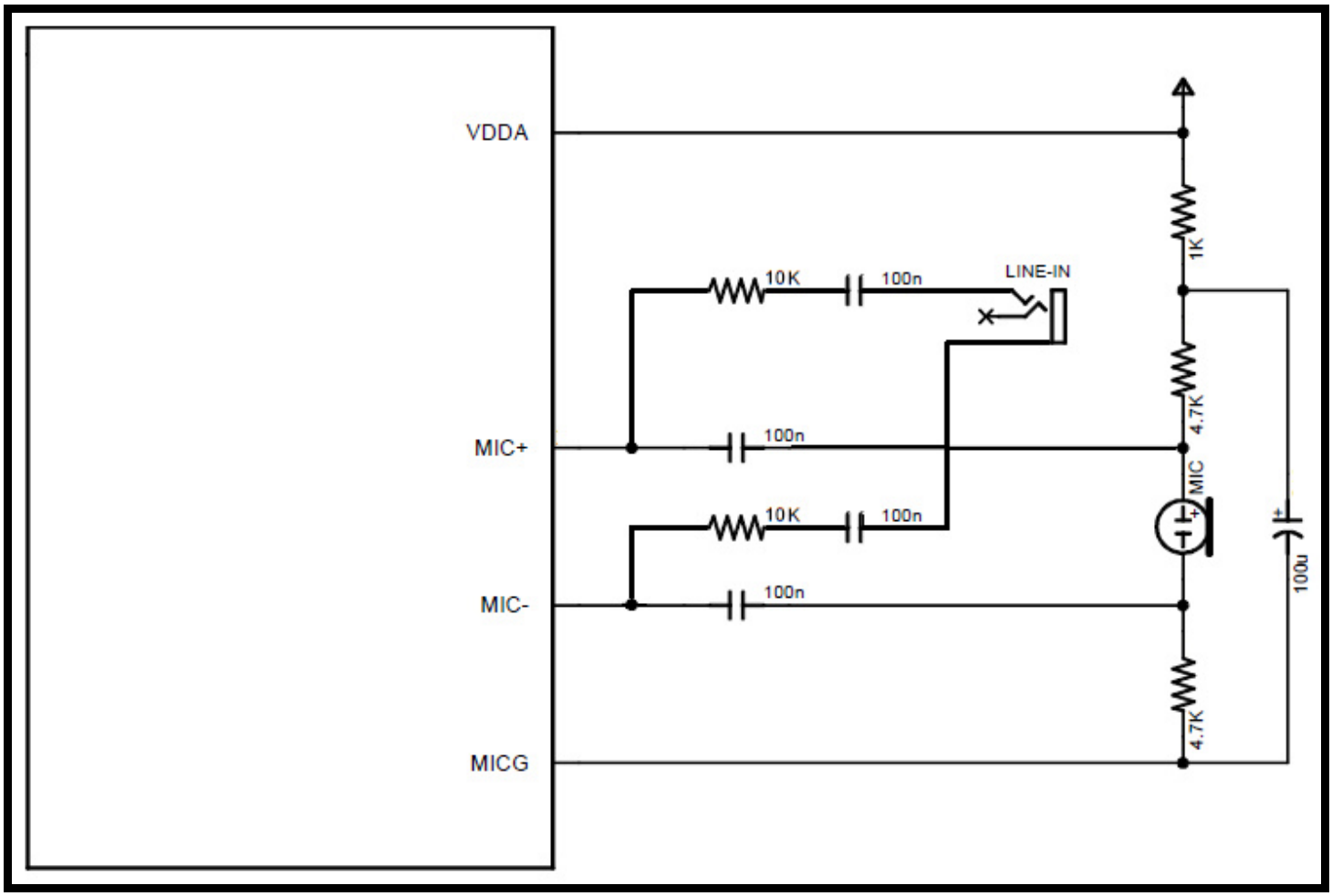


(A) Microphone



Note: The 10K resistor used for input signal adjust, and the value just for reference.

(B) Line-In



Note: The 10K resistor used for input signal adjust, and the value just for reference.

(C) Microphone + Line-In

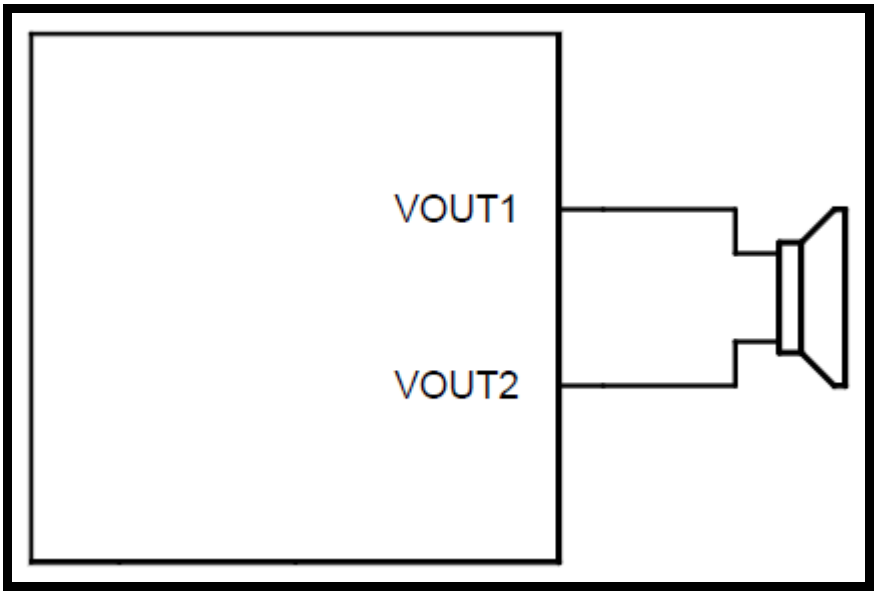
■ VOICE OUTPUT

The aPR2060 support 2 voice output mode, PWM and DAC.

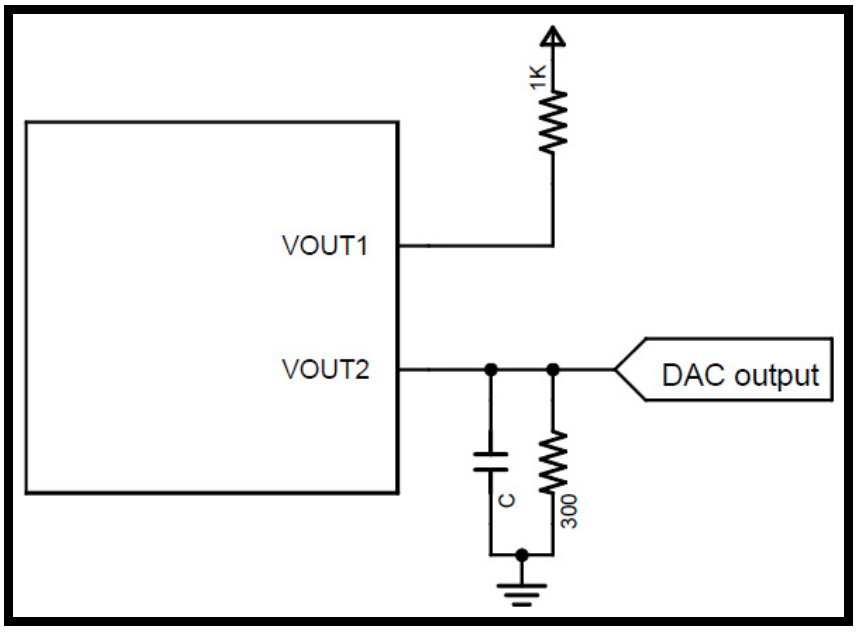
The PWM mode use VOUT1 and VOUT2 pin to drive speaker directly without external components to save cost.

The DAC mode use VOUT2 pin to output current signal. User can use the signal to drive audio amplifier or mix with other components in their applications to provide larger voice volume.

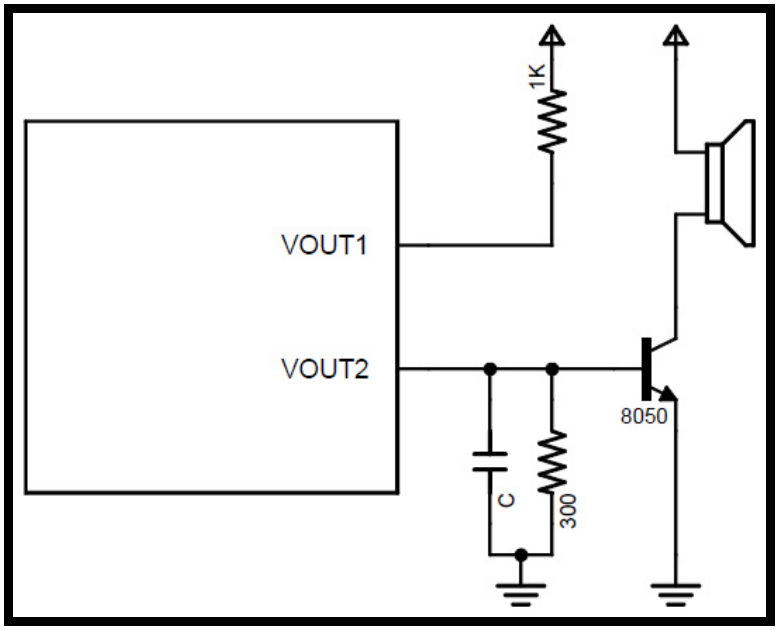
The following fig. show circuit for different output methods: PWM, DAC, DAC with transistor, DAC with audio amplifier AP4890B.



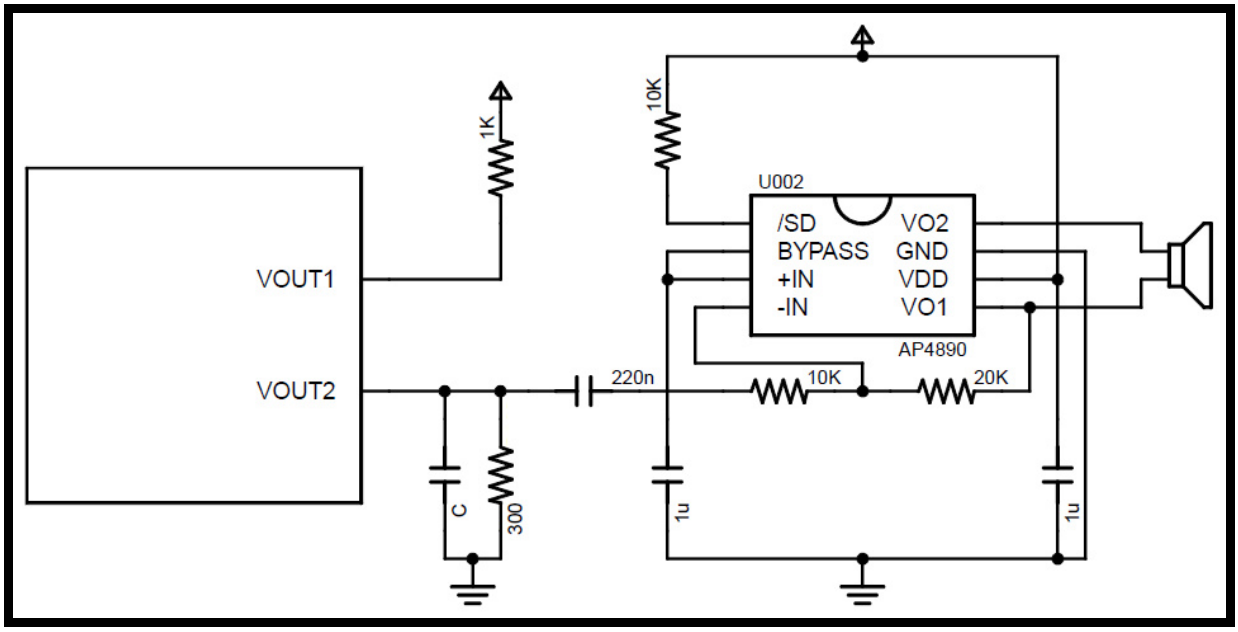
(A) PWM



(B) DAC



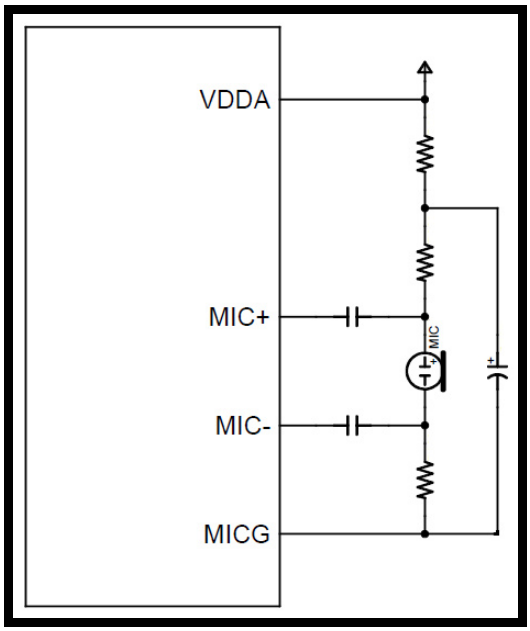
(C) DAC with transistor



(D) DAC with audio amplifier AP4890B

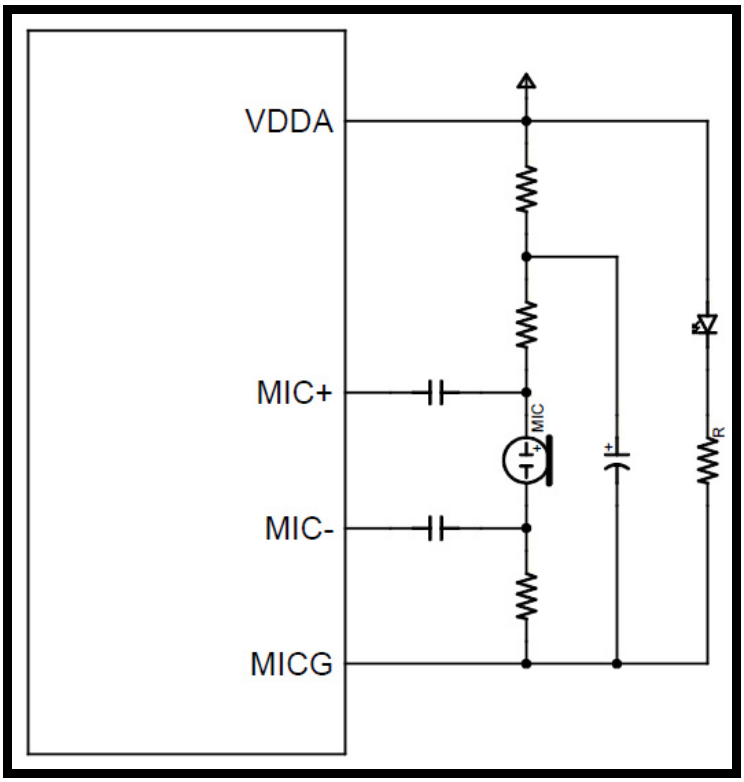
■ BUSY

The MICG pin will be drove to low during the message record or playback, and drove to high during idle or standby, user can detect MICG status to know chip is busy or not.

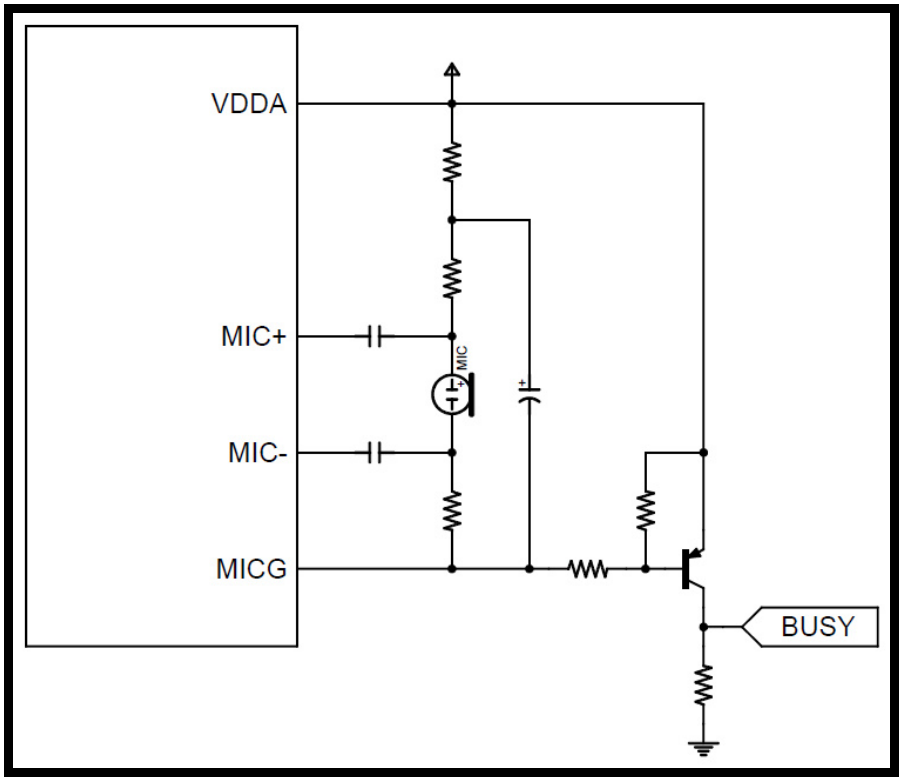


Please note it is limited for MICG pin driving current. Reference to I_{OH} and I_{OL} in section "**DC CHARACTERISTICS"**. If MICG pin is over loading from external circuit, it will cause noise in microphone circuit.

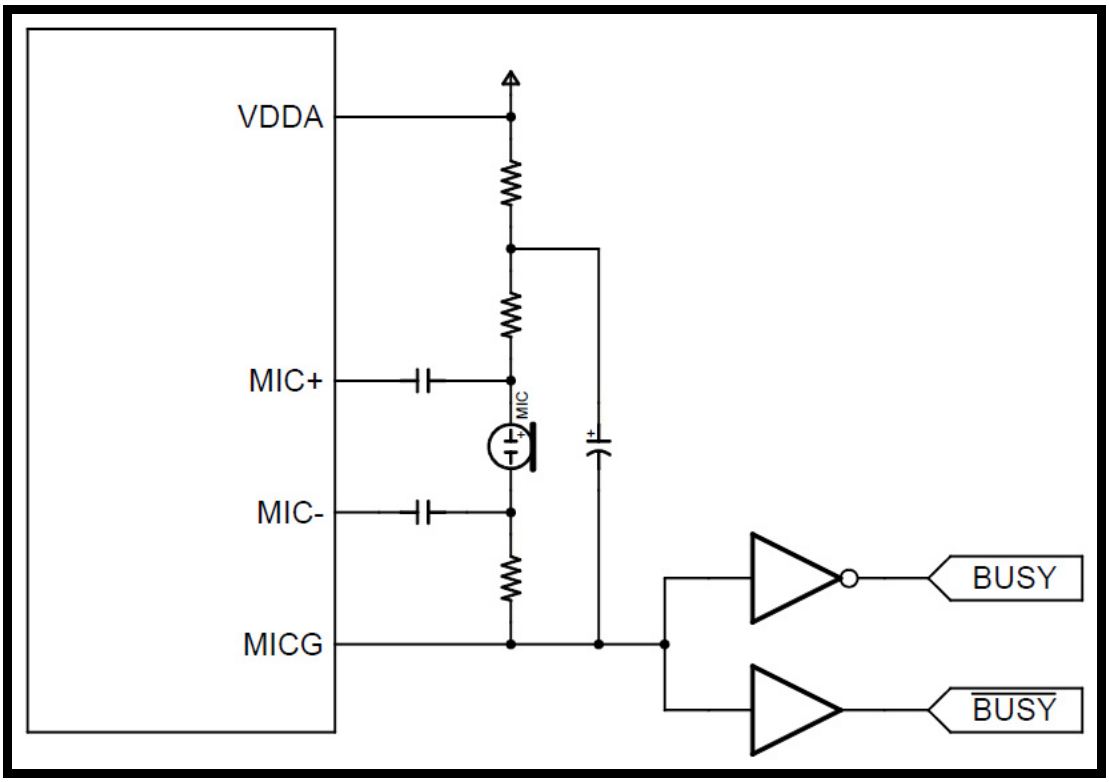
Below is a typical application. We add one LED to indicate IC record and playback status. We use one Resistor to limit current. And suggest R> 470Ω



Below Transistor circuit is to get higher current, larger than I_{OH} or I_{OL}.



To get best sound quality, we can use buffer or inverter to isolate MICG to avoid noise from external circuit. Driving current is provided by buffer(inverter) only.

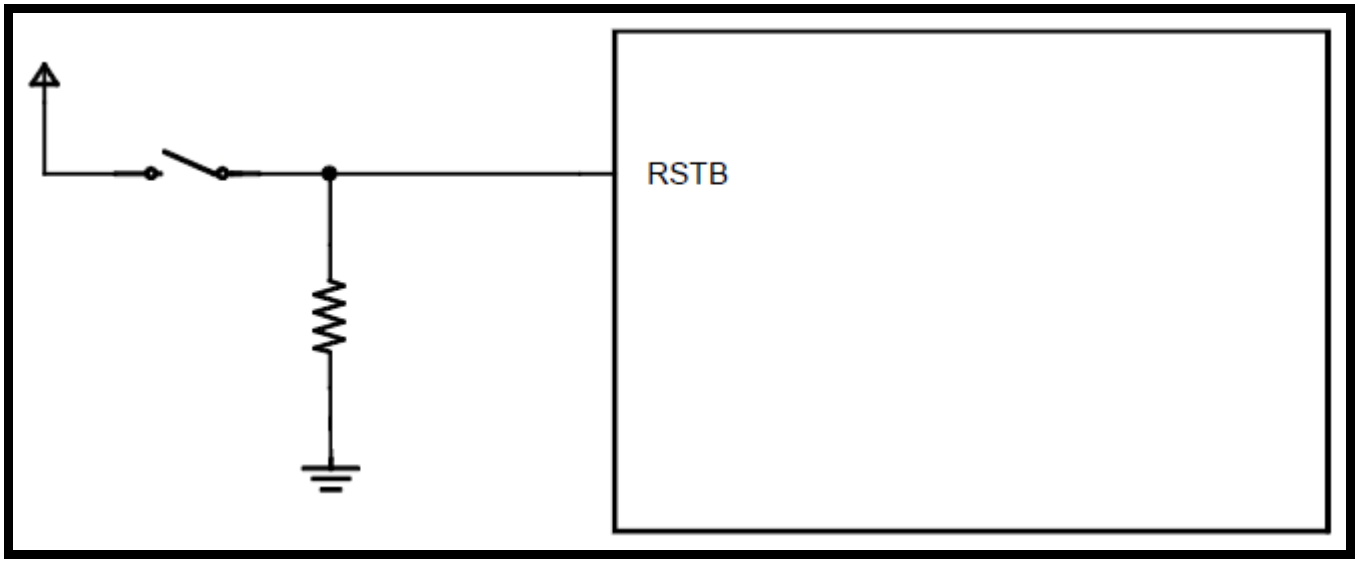


■ RESET

The aPR2060 can enter standby mode when RSTB pin drive to low. During chip in the standby mode, the current consumption is reduced to I_{SB} and any operation will be stopped, user also can not execute any new operate in this mode.

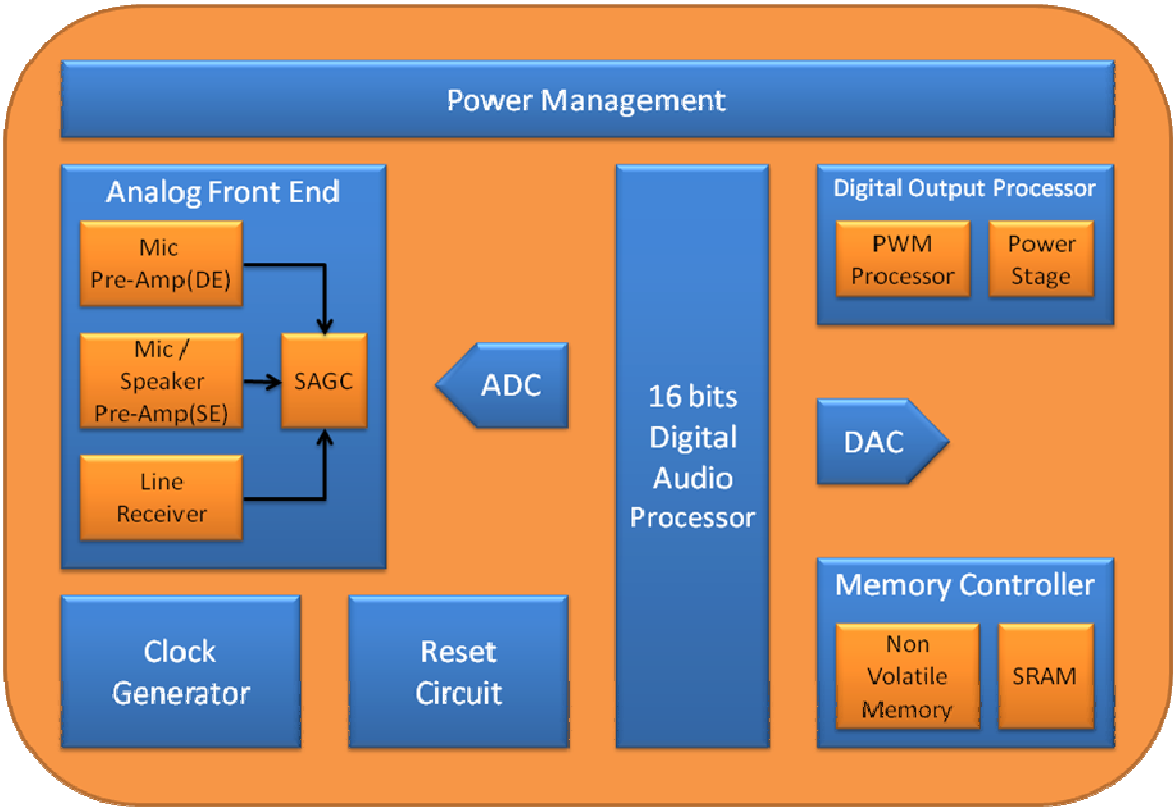
The standby mode will continue until RSTB pin goes to high, chip will be started to initial, and playback “beep” tone to indicate enter idle mode.

User can get less current consumption by control RSTB pin specially in some application which concern standby current.



■ BLOCK DIAGRAM

Figure 1. Block Diagram



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Unit
VDD – VSS	-0.3 ~ +10.0	V
V_{IN}	VSS-0.3 < V_{IN} < VDD+0.3	V
V_{OUT}	VSS < V_{OUT} < VDD	V
T(Operating)	-40 ~ +85	℃
T(Junction)	-40 ~ +125	℃
T(Storage)	-40 ~ +125	℃

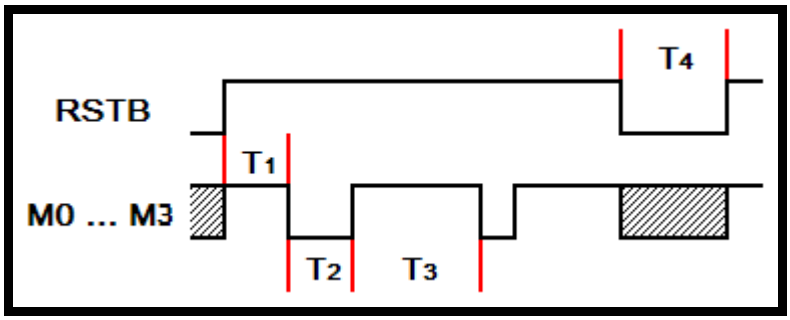
■ DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VDD	Operating Voltage	3.0		6.5	V	
I_{SB}	Standby Current			1	μA	
I_{PDN}	Power-Down Current		10		μA	
$I_{OP(IDLE)}$	Operating Current (Idle)		20		mA	VDD = 5V
$I_{OP(REC)}$	Operating Current (Record)		35		mA	VDD = 5V
$I_{OP(PLAY)}$	Operating Current (Playback)		25		mA	VDD = 5V
V_{IH}	"H" Input Voltage	2.5			V	
V_{IL}	"L" Input Voltage			0.6	V	
I_{VOUT}	VOUT Current		185		mA	
I_{OH}	O/P High Current		8		mA	VDD = 5V / VOH=4.5V
I_{OL}	O/P Low Current		14		mA	VDD = 5V / VOH=0.5V
R_{NPIO}	Input pin pull-down resistance		300		KΩ	External floating or drive low.
			1		MΩ	External drive high.
R_{UPIO}	Input pin pull-up resistance		4.7		KΩ	
△Fs/Fs	Frequency stability			5	%	VDD = 5V ± 1.0V
△Fc/Fc	Chip to chip Frequency Variation			5	%	Also apply to lot to lot variation.

■ SAMPLES RATES & RESISTANCE VALUES (for reference only)

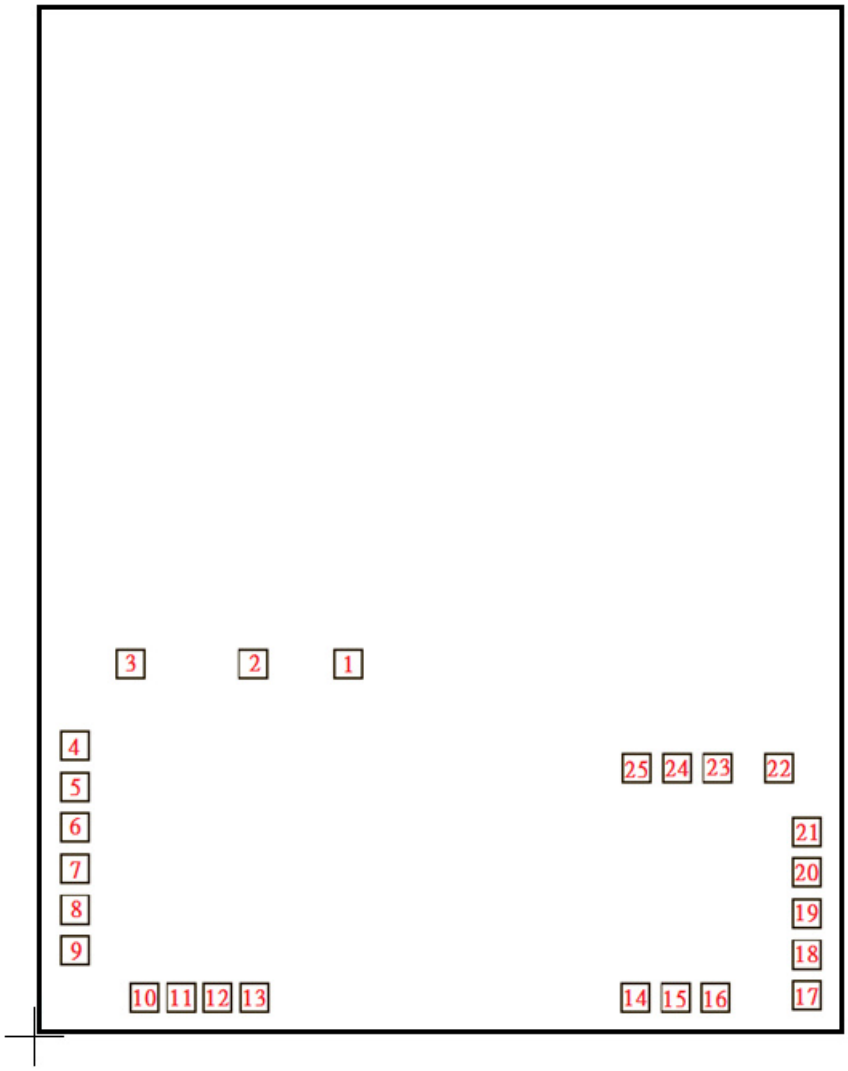
Sample Rate	Seconds	Resistance
12KHz	42 sec	47K
11KHz	46 sec	63K
10KHz	51 sec	79K
9KHz	56 sec	100K
8KHz	64 sec	120K
7KHz	73 sec	143K
6KHz	85 sec	173K

■ AC CHARACTERISTICS



Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T1	System Initial Time	100	--	--	mS	VDD=5.0V
T2	Trigger Setup Time	16	--	--	mS	VDD=5.0V
T3	Trigger Hold Time	16	--	--	mS	VDD=5.0V
T4	Reset Hold Time	100	--	--	uS	VDD=5.0V

■ BONDING PAD DIAGRAMS

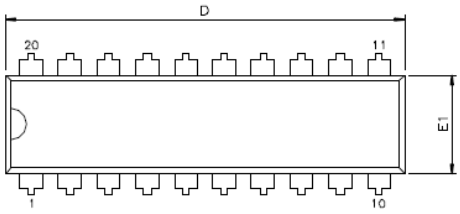


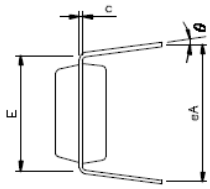
Die Size	2400 X 3000						
Pad Windows	80 X 80						
Pad No	Pad Name	Pad Location		Pad No	Pad Name	Pad Location	
		X	Y			X	Y
1	VSSL	920	1080	14	VDDA	1780	101
2	VCORE	635	1080	15	RSTB	1900	101
3	N.C.	270	1080	16	VREF	2020	101
4	ROSC	102.4	840	17	N.C.	2293.6	108
5	N.C.	102.4	720	18	M3/MSEL1	2293.6	228
6	M0	102.4	600	19	M1	2293.6	348
7	M2/MSEL0	102.4	480	20	/REC	2293.6	468
8	N.C.	102.4	360	21	MICG	2293.6	588
9	VSSP	102.4	240	22	VSSA	2210	775
10	VOUT1	310	101	23	VCM	2025	775
11	VOUT2	420	101	24	MIC+	1905	775
12	VDDL	530	101	25	MIC-	1785	775
13	VDDP	640	101				

Unit: um

PACKAGES DIMENSION OUTLINES

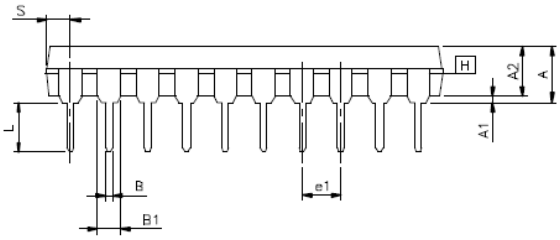
20-Pin 300mil DIP Package





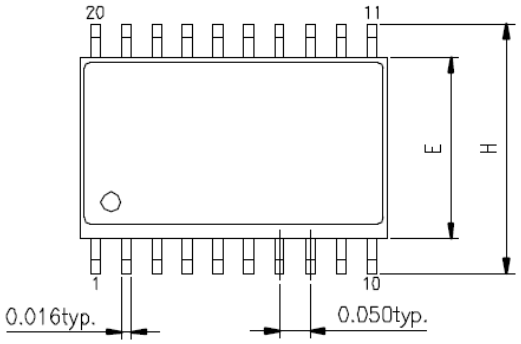
SYMBOLS	MIN	NOM	MAX
A	–	–	0.175
A1	0.015	–	–
A2	0.125	0.130	0.135
B	0.016	0.018	0.020
B1	0.058	0.060	0.064
c	0.008	0.010	0.011
D	1.012	1.026	1.040
E	0.290	0.300	0.310
E1	0.245	0.250	0.255
e1	0.090	0.100	0.110
L	0.120	0.130	0.140
θ	0	–	15
eA	0.335	0.355	0.375
S	–	–	0.075

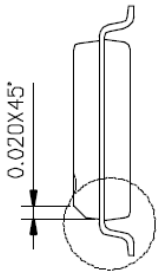
UNIT : INCH



NOTES:
1. JEDEC OUTLINE : MS-001 AD
2. "D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. eA IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM.
6. DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

20-Pin 300mil SOP Package

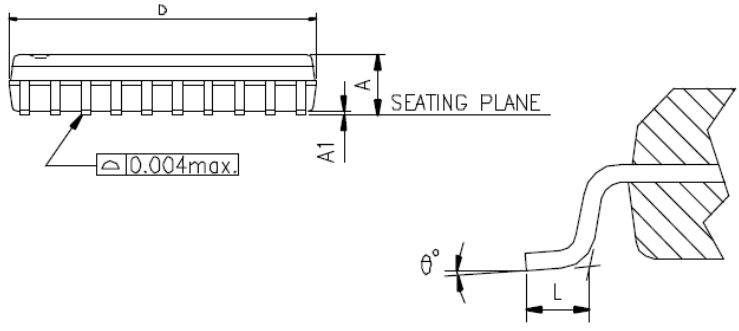




SYMBOLS	MIN.	MAX.
A	0.093	0.104
A1	0.004	0.012
D	0.496	0.508
E	0.291	0.299
H	0.394	0.419
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1. JEDEC OUTLINE : MS-013 AC
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.



■ HISTORY

Ver. A (2014/05/22)

- Original version data sheet for aPR2060 T2.2.