

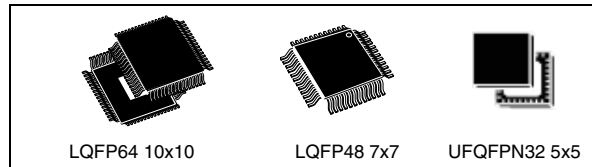


# STM32F051x4 STM32F051x6 STM32F051x8

Low- and medium-density advanced ARM™-based 32-bit MCU with 16 to 64 Kbytes Flash, timers, ADC, DAC and comm. interfaces

## Features

- Operating conditions:
  - Voltage range: 2.0 V to 3.6 V
- ARM 32-bit Cortex®-M0 CPU (48 MHz max)
- Memories
  - 16 to 64 Kbytes of Flash memory
  - 8 Kbytes of SRAM with HW parity checking
- CRC calculation unit
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x6 PLL option
  - Internal 40 kHz RC oscillator
- Calendar RTC with alarm and periodic wakeup from Stop/Standby
- Reset and supply management
  - Power-on/Power down reset (POR/PDR)
  - Programmable voltage detector (PVD)
- Low power Sleep, Stop, and Standby modes
- V<sub>BAT</sub> supply for RTC and backup registers
- 5-channel DMA controller
- 1 × 12-bit, 1.0 μs ADC (up to 16 channels)
  - Conversion range: 0 to 3.6V
  - Separate analog supply from 2.4 up to 3.6
- Two fast low-power analog comparators with programmable input and output
- One 12-bit D/A converter
- Up to 55 fast I/Os
  - All mappable on external interrupt vectors
  - Up to 36 I/Os with 5 V tolerant capability
- Up to 18 capacitive sensing channels supporting touchkey, linear and rotary touch sensors
- 96-bit unique ID
- Serial wire debug (SWD)



- Up to 11 timers
  - One 16-bit 7-channel advanced-control timer for 6 channels PWM output, with deadtime generation and emergency stop
  - One 32-bit and one 16-bit timer, with up to 4 IC/OC, usable for IR control decoding
  - One 16-bit timer, with 2 IC/OC, 1 OCN, deadtime generation and emergency stop
  - Two 16-bit timers, each with IC/OC and OCN, deadtime generation, emergency stop and modulator gate for IR control
  - One 16-bit timer with 1 IC/OC
  - Independent and system watchdog timers
  - SysTick timer: 24-bit downcounter
  - One 16-bit basic timer to drive the DAC
- Communication interfaces
  - Up to two I<sup>2</sup>C interfaces; one supporting Fast Mode Plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus, and wakeup from STOP
  - Up to two USARTs supporting master synchronous SPI and modem control; one with ISO7816 interface, LIN, IrDA capability, auto baud rate detection and wakeup feature
  - Up to two SPIs (18 Mbit/s) with 4 to 16 programmable bit frame, 1 with I<sup>2</sup>S interface multiplexed
  - HDMI CEC interface, wakeup on header reception

**Table 1. Device summary**

| Reference   | Part number                           |
|-------------|---------------------------------------|
| STM32F051x4 | STM32F051K4, STM32F051C4, STM32F051R4 |
| STM32F051x6 | STM32F051K6, STM32F051C6, STM32F051R6 |
| STM32F051x8 | STM32F051C8, STM32F051R8, STM32F051K8 |

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# 1 Description

The STM32F051xx family incorporates the high-performance ARM Cortex™-M0 32-bit RISC core operating at a 48 MHz frequency, high-speed embedded memories (Flash memory up to 64 Kbytes and SRAM up to 8 Kbytes), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (up to two I<sup>2</sup>Cs, two SPIs, one I2S, one HDMI CEC, and up to two USARTs), one 12-bit ADC, one 12-bit DAC, up to five general-purpose 16-bit timers, a 32-bit timer and an advanced-control PWM timer.

The STM32F051xx family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F051xx family includes devices in three different packages ranging from 32 pins to 64 pins. Depending on the device chosen, different sets of peripherals are included. The description below provides an overview of the complete range of peripherals proposed in this family.

These features make the STM32F051xx microcontroller family suitable for a wide range of applications such as application control and user interfaces, handheld equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

**Table 2. STM32F051xx family device features and peripheral counts**

| Peripheral                                   |                          | STM32F051Kx   |    |      | STM32F051Cx         |    |      | STM32F051Rx             |    |      |
|--|--------------------------|---|----|------|---------------------|----|------|-------------------------|----|------|
| Flash (Kbytes)                               |                          | 16  | 32 | 64   | 16                  | 32 | 64   | 16                      | 32 | 64   |
| SRAM (Kbytes)                                |                          | 4   |    | 8    | 4                   |    | 8    | 4                       |    | 8    |
| Timers                                       | Advanced control         | 1 (16-bit)  |    |      |                     |    |      |                         |    |      |
|  | General purpose          | 5 (16-bit)<br>1 (32-bit)  |    |      |                     |    |      |                         |    |      |
|  | Basic                    | 1 (16-bit)  |    |      |                     |    |      |                         |    |      |
| Comm. interfaces                             | SPI (I2S) <sup>(1)</sup> | 1(1) <sup>(2)</sup>   |    | 2(1) | 1(1) <sup>(2)</sup> |    | 2(1) | 1(1) <sup>(2)</sup>     |    | 2(1) |
|  | I <sup>2</sup> C         | 1 <sup>(3)</sup>  |    | 2    | 1 <sup>(3)</sup>    |    | 2    | 1 <sup>(3)</sup>        |    | 2    |
|  | USART                    | 1 <sup>(4)</sup>  | 2  |      | 1 <sup>(4)</sup>    | 2  |      | 1 <sup>(4)</sup>        | 2  |      |
|  | CEC                      | 1   |    |      |                     |    |      |                         |    |      |
| 12-bit synchronized ADC (number of channels) |                          | 1<br>(10 ext. + 3 int.)   |    |      |                     |    |      | 1<br>(16 ext. + 3 int.) |    |      |
| GPIOs  |                          | 27  |    |      | 39                  |    |      | 55                      |    |      |
| Capacitive sensing channels                  |                          | 14  |    |      | 17                  |    |      | 18                      |    |      |
| 12-bit DAC (number of channels)              |                          | 1<br>(1)  |    |      |                     |    |      |                         |    |      |
| Analog comparator                            |                          | 2   |    |      |                     |    |      |                         |    |      |
| Max. CPU frequency                           |                          | 48 MHz  |    |      |                     |    |      |                         |    |      |
| Operating voltage                            |                          | 2.0 to 3.6 V  |    |      |                     |    |      |                         |    |      |
| Operating temperature                        |                          | Ambient operating temperature: -40 °C to 85 °C / -40 °C to 105 °C<br>Junction temperature: -40 °C to 125 °C |    |      |                     |    |      |                         |    |      |
| Packages                                     |                          | UFQFPN32  |    |      | LQFP48              |    |      | LQFP64                  |    |      |

1. The SPI1 interface can be used either in SPI mode or in I2S audio mode.
2. SPI2 is not present
3. I2C2 is not present
4. USART2 is not present

## 2 Device overview

Figure 1. Block diagram

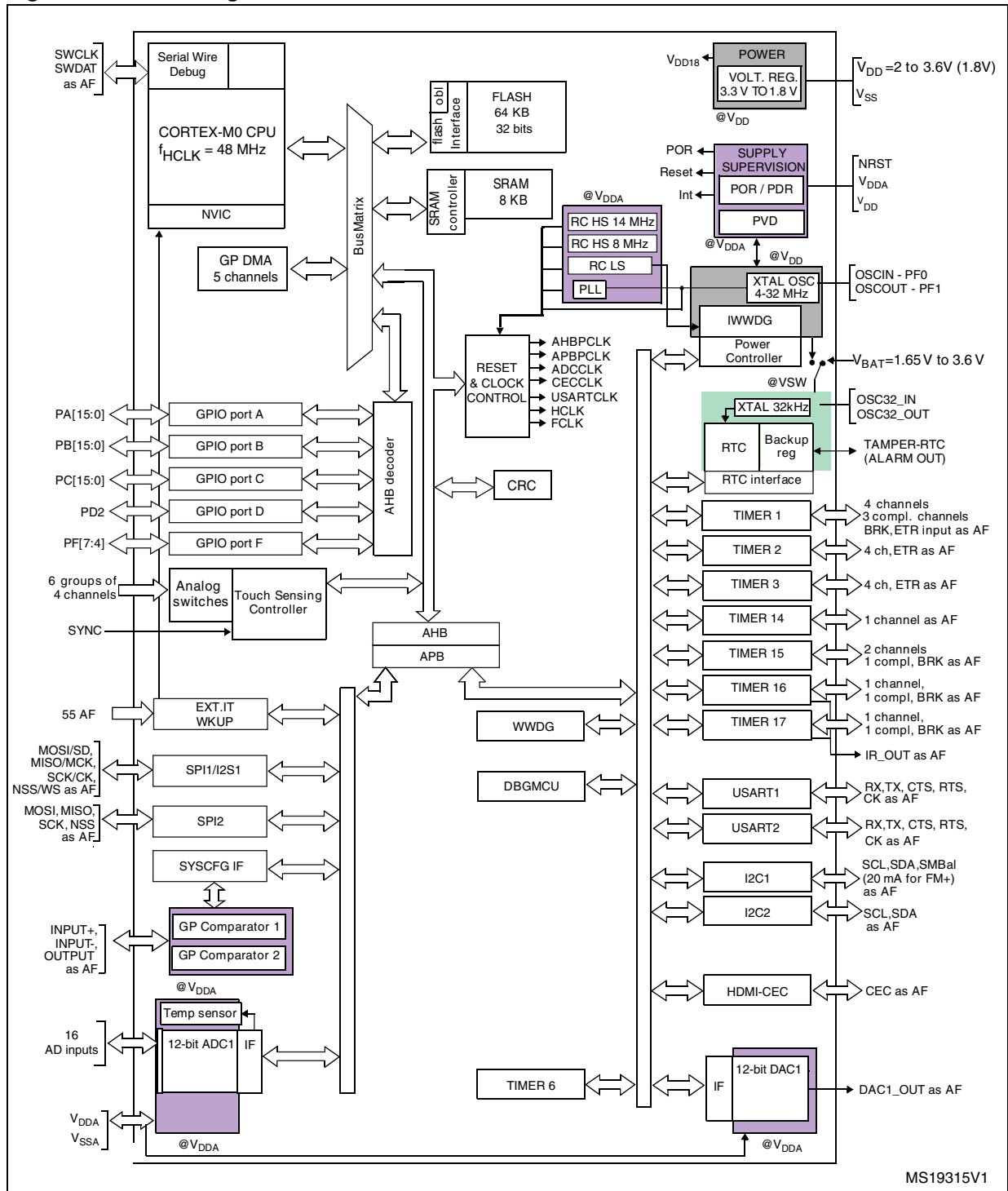
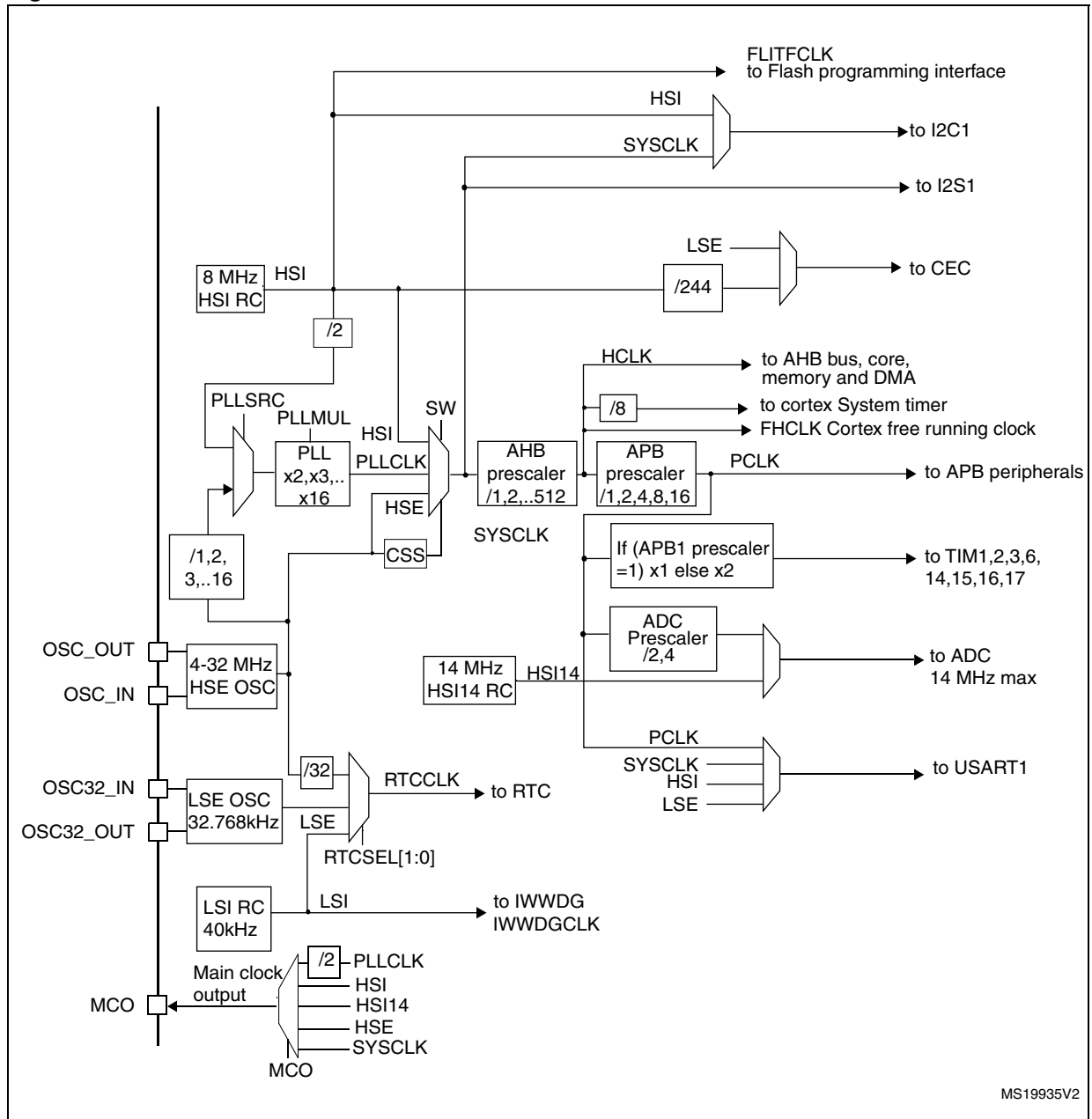




Figure 2. Clock tree



## 3 Functional overview

### 3.1 ARM<sup>®</sup> Cortex<sup>™</sup>-M0 core with embedded Flash and SRAM

The ARM Cortex<sup>™</sup>-M0 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex<sup>™</sup>-M0 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F051xx family has an embedded ARM core and is therefore compatible with all ARM tools and software.

*Figure 1* shows the general block diagram of the device family.

### 3.2 Memories

The device has the following features:

- Up to 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 16 to 64 Kbytes of embedded Flash memory for programs and data
  - Option bytes

The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features (Cortex-M0 serial wire) and boot in RAM selection disabled

### 3.3 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 96-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

### 3.4 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPI, I2S, I2C, USART, all TIMx timers (except TIM14), DAC and ADC.

### 3.5 Nested vectored interrupt controller (NVIC)

The STM32F051xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M0) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

### 3.6 Extended interrupt/event controller (EXTI)

The external interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 55 GPIOs can be connected to the 16 external interrupt lines.

## 3.7 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

## 3.8 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1.

## 3.9 Power management

### 3.9.1 Power supply schemes

- $V_{DD} = 2.0$  to  $3.6$  V: external power supply for I/Os and the internal regulator. Provided externally through  $V_{DD}$  pins.
- $V_{DDA} = 2.0$  to  $3.6$  V: external analog power supply for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to  $V_{DDA}$  is  $2.4$  V when the ADC and DAC are used). The  $V_{DDA}$  voltage level must be always greater or equal to the  $V_{DD}$  voltage level and must be provided first.
- $V_{BAT} = 1.6$  to  $3.6$  V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when  $V_{DD}$  is not present.

For more details on how to connect power pins, refer to [Figure 9: Power supply scheme](#).

### 3.9.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold,  $V_{POR/PDR}$ , without the need for an external reset circuit.

- The POR monitors only the  $V_{DD}$  supply voltage. During the startup phase it is required that  $V_{DDA}$  should arrive first and be greater than or equal to  $V_{DD}$ .
- The PDR monitors both the  $V_{DD}$  and  $V_{DDA}$  supply voltages, however the  $V_{DDA}$  power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that  $V_{DDA}$  is higher than or equal to  $V_{DD}$ .

The device features an embedded programmable voltage detector (PVD) that monitors the  $V_{DD}$  power supply and compares it to the  $V_{PVD}$  threshold. An interrupt can be generated when  $V_{DD}$  drops below the  $V_{PVD}$  threshold and/or when  $V_{DD}$  is higher than the  $V_{PVD}$  threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.9.3 Voltage regulator

The regulator has three operating modes: main (MR), low power (LPR) and power down.

- MR is used in normal operating mode (Run)
- LPR can be used in Stop mode where the power demand is reduced
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

## 3.10 Low-power modes

The STM32F051xx family supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC alarm, COMPx, I2C1, USART1 or the CEC.

The I2C1, USART1 and the CEC can be configured to enable the HSI RC oscillator for processing incoming data. If this is used, the voltage regulator should not be put in the low-power mode but kept in normal mode.

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pins, or an RTC alarm occurs.

*Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

### 3.11 Real-time clock (RTC) and backup registers

The RTC and the 5 backup registers are supplied through a switch that takes power either on  $V_{DD}$  supply when present or through the  $V_{BAT}$  pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when  $V_{DD}$  power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month.
- Programmable alarm with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

## 3.12 Timers and watchdogs

The STM32F051xx family devices include up to six general-purpose timers, one basic timer and an advanced control timer.

[Table 3](#) compares the features of the advanced-control, general-purpose and basic timers.

**Table 3. Timer feature comparison**

| Timer type       | Timer        | Counter resolution | Counter type      | Prescaler factor                | DMA request generation | Capture/compare channels | Complementary outputs |
|------------------|--------------|--------------------|-------------------|---------------------------------|------------------------|--------------------------|-----------------------|
| Advanced control | TIM1         | 16-bit             | Up, down, up/down | Any integer between 1 and 65536 | Yes                    | 4                        | Yes                   |
| General purpose  | TIM2         | 32-bit             | Up, down, up/down | Any integer between 1 and 65536 | Yes                    | 4                        | No                    |
|                  | TIM3         | 16-bit             | Up, down, up/down | Any integer between 1 and 65536 | Yes                    | 4                        | No                    |
|                  | TIM14        | 16-bit             | Up                | Any integer between 1 and 65536 | No                     | 1                        | No                    |
|                  | TIM15        | 16-bit             | Up                | Any integer between 1 and 65536 | Yes                    | 2                        | Yes                   |
|                  | TIM16, TIM17 | 16-bit             | Up                | Any integer between 1 and 65536 | Yes                    | 1                        | Yes                   |
| Basic            | TIM6         | 16-bit             | Up                | Any integer between 1 and 65536 | Yes                    | 0                        | No                    |

### 3.12.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

### 3.12.2 General-purpose timers (TIM2..3, TIM14..17)

There are six synchronizable general-purpose timers embedded in the STM32F051xx devices (see [Table 3](#) for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

#### TIM2, TIM3

STM32F051xx devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

#### TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

#### TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16, and TIM17 have a complementary output with dead-time generation and independent DMA request generation

Their counters can be frozen in debug mode.

### 3.12.3 Basic timer TIM6

This timer is mainly used for DAC trigger generation. It can also be used as a generic 16-bit time base.



### 3.12.4 Independent window watchdog (IWWDG)

The independent window watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### 3.12.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 3.12.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source (HCLK or HCLK/8)

## 3.13 Inter-integrated circuit interfaces (I<sup>2</sup>C)

Up to two I<sup>2</sup>C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s) or Fast mode (up to 400 kbit/s) and I2C1 supports also Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

**Table 4. Comparison of I2C analog and digital filters**

|                                  | Analog filter   | Digital filter   |
|----------------------------------|---|--|
| Pulse width of suppressed spikes | ≥ 50 ns   | Programmable length from 1 to 15 I2C peripheral clocks                       |
| Benefits                         | Available in Stop mode                                | 1. Extra filtering capability vs. standard requirements.<br>2. Stable length |
| Drawbacks                        | Variations depending on temperature, voltage, process | Disabled when Wakeup from Stop mode is enabled                               |

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C interfaces can be served by the DMA controller.

Refer to [Table 5](#) for the differences between I2C1 and I2C2.

**Table 5. STM32F051xx I<sup>2</sup>C implementation**

| I2C features <sup>(1)</sup>                                 | I2C1 | I2C2 |
|---|------|------|
| 7-bit addressing mode                                       | X    | X    |
| 10-bit addressing mode                                      | X    | X    |
| Standard mode (up to 100 kbit/s)                            | X    | X    |
| Fast mode (up to 400 kbit/s)                                | X    | X    |
| Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s) | X    |      |
| Independent clock   | X    |      |
| SMBus   | X    |      |
| Wakeup from STOP  | X    |      |

1. X = supported.

### 3.14 Universal synchronous/asynchronous receiver transmitters (USART)

The device embeds up to two universal synchronous/asynchronous receiver transmitters (USART1 and USART2), which communicate at speeds of up to 6 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. The USART1 supports also SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock, allowing the USART1 to wake up the MCU from Stop mode.

The USART interfaces can be served by the DMA controller. Serial peripheral interface (SPI).

Refer to [Table 6](#) for the differences between USART1 and USART2.

**Table 6. STM32F051xx USART implementation**

| USART modes/features <sup>(1)</sup>         | USART1 | USART2 |
|---|--------|--------|
| Hardware flow control for modem             | X      | X      |
| Continuous communication using DMA          | X      | X      |
| Multiprocessor communication                | X      | X      |
| Synchronous mode                            | X      | X      |
| Smartcard mode                              | X      |        |
| Single-wire half-duplex communication       | X      | X      |
| IrDA SIR ENDEC block                        | X      |        |
| LIN mode                                    | X      |        |
| Dual clock domain and wakeup from Stop mode | X      |        |
| Receiver timeout interrupt                  | X      |        |
| Modbus communication                        | X      |        |
| Auto baud rate detection                    | X      |        |
| Driver Enable                               | X      | X      |

1. X = supported.

### 3.15 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I<sup>2</sup>S)

Up to two SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

One standard I<sup>2</sup>S interface (multiplexed with SPI1) supporting four different audio standards can operate as master or slave at simplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

Refer to [Table 7](#) for the differences between SPI1 and SPI2.

**Table 7. STM32F051x SPI/I<sup>2</sup>S implementation**

| SPI features <sup>(1)</sup> | SPI1 | SPI2 |
|-----------------------------|------|------|
| Hardware CRC calculation    | X    | X    |
| Rx/Tx FIFO                  | X    | X    |
| NSS pulse mode              | X    | X    |
| I <sup>2</sup> S mode       | X    |      |
| TI mode                     | X    | X    |

1. X = supported.

### 3.16 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI\_CEC controller to wakeup the MCU from Stop mode on data reception.

### 3.17 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

### 3.18 Touch sensing controller (TSC)

The device has an embedded independent hardware controller (TSC) for controlling touch sensing acquisitions on the I/Os.

Up to 18 touch sensing electrodes can be controlled by the TSC. The touch sensing I/Os are organized in 6 acquisition groups, with up to 4 I/Os in each group.

**Table 8. Capacitive sensing GPIOs available on STM32F051x devices**

| Group | Capacitive sensing signal name | Pin name | Group | Capacitive sensing signal name | Pin name |
|-------|--------------------------------|----------|-------|--------------------------------|----------|
| 1     | TSC_G1_IO1                     | PA0      | 4     | TSC_G4_IO1                     | PA9      |
|       | TSC_G1_IO2                     | PA1      |       | TSC_G4_IO2                     | PA10     |
|       | TSC_G1_IO3                     | PA2      |       | TSC_G4_IO3                     | PA11     |
|       | TSC_G1_IO4                     | PA3      |       | TSC_G4_IO4                     | PA12     |
| 2     | TSC_G2_IO1                     | PA4      | 5     | TSC_G5_IO1                     | PB3      |
|       | TSC_G2_IO2                     | PA5      |       | TSC_G5_IO2                     | PB4      |
|       | TSC_G2_IO3                     | PA6      |       | TSC_G5_IO3                     | PB6      |
|       | TSC_G2_IO4                     | PA7      |       | TSC_G5_IO4                     | PB7      |
| 3     | TSC_G3_IO1                     | PB0      | 6     | TSC_G6_IO1                     | PB11     |
|       | TSC_G3_IO2                     | PB1      |       | TSC_G6_IO2                     | PB12     |
|       | TSC_G3_IO3                     | PB2      |       | TSC_G6_IO3                     | PB13     |
|       | TSC_G3_IO4                     | PC5      |       | TSC_G6_IO4                     | PB14     |

**Table 9. No. of capacitive sensing channels available on STM32F051xx devices**

| Analog I/O group                      | Number of capacitive sensing channels |             |             |
|---------------------------------------|---------------------------------------|-------------|-------------|
|                                       | STM32F051Rx                           | STM32F051Cx | STM32F051Kx |
| G1                                    | 3                                     | 3           | 3           |
| G2                                    | 3                                     | 3           | 3           |
| G3                                    | 3                                     | 2           | 2           |
| G4                                    | 3                                     | 3           | 3           |
| G5                                    | 3                                     | 3           | 3           |
| G6                                    | 3                                     | 3           | 0           |
| Number of capacitive sensing channels | 18                                    | 17          | 14          |

### 3.19 Analog to digital converter (ADC)

The 12-bit analog to digital converter has up to 16 external and 3 internal (temperature sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

#### 3.19.1 Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. The conversion range is between  $2\text{ V} < V_{\text{DDA}} < 3.6\text{ V}$ . The temperature sensor is internally connected to the ADC\_IN16 input channel which is used to convert the sensor output voltage into a digital value.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

#### 3.19.2 V<sub>BAT</sub> battery voltage monitoring

This embedded hardware feature allows the application to measure the V<sub>BAT</sub> battery voltage using the internal ADC channel ADC\_IN18. As the V<sub>BAT</sub> voltage may be higher than V<sub>DDA</sub>, and thus outside the ADC input range, the V<sub>BAT</sub> pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V<sub>BAT</sub> voltage.

## 3.20 Digital-to-analog converter (DAC)

The 12-bit buffered DAC channel can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This digital Interface supports the following features:

- Left or right data alignment in 12-bit mode
- Synchronized update capability
- DMA capability
- External triggers for conversion

Five DAC trigger inputs are used in the device. The DAC is triggered through the timer trigger outputs and the DAC interface is generating its own DMA requests.

## 3.21 Fast low power comparators and reference voltage

The device embeds two fast rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pin
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to [Table 21: Embedded internal reference voltage](#) for the value and precision of the internal reference voltage.

Both comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

The internal voltage reference is also connected to ADC\_IN17 input channel of the ADC.

### 3.21.1 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

# 4 Pinouts and pin description

Figure 3. LQFP64 64-pin package pinout

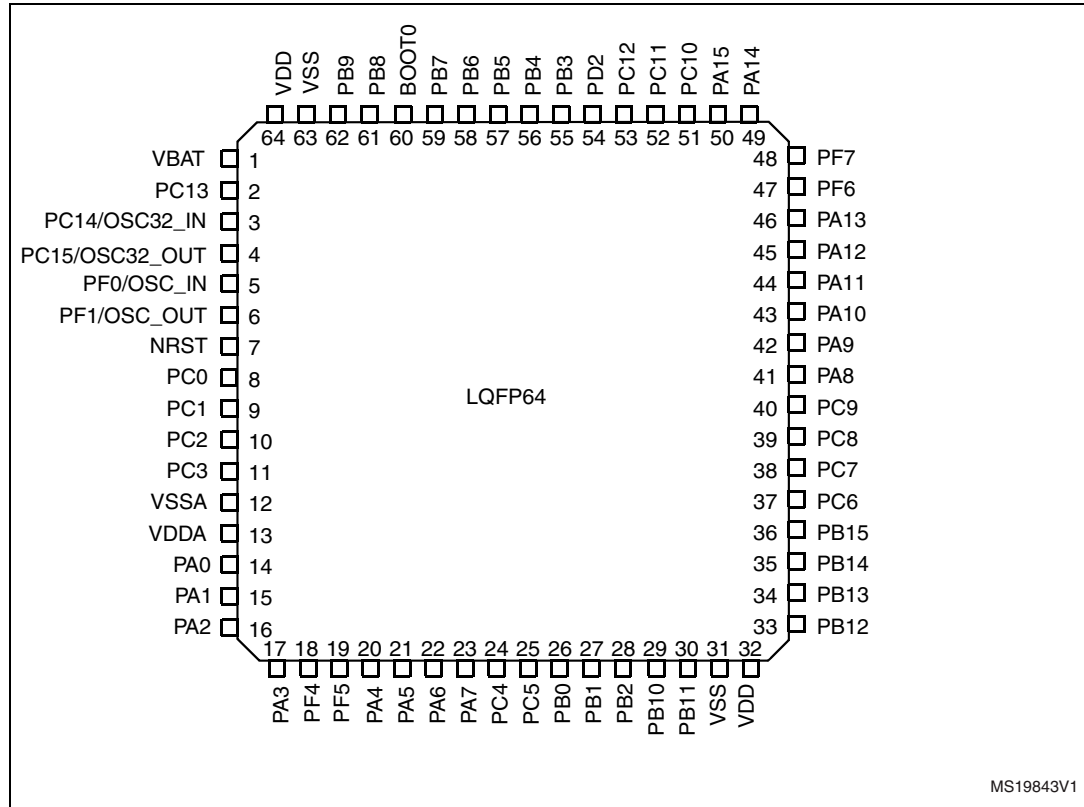


Figure 4. LQFP48 48-pin package pinout

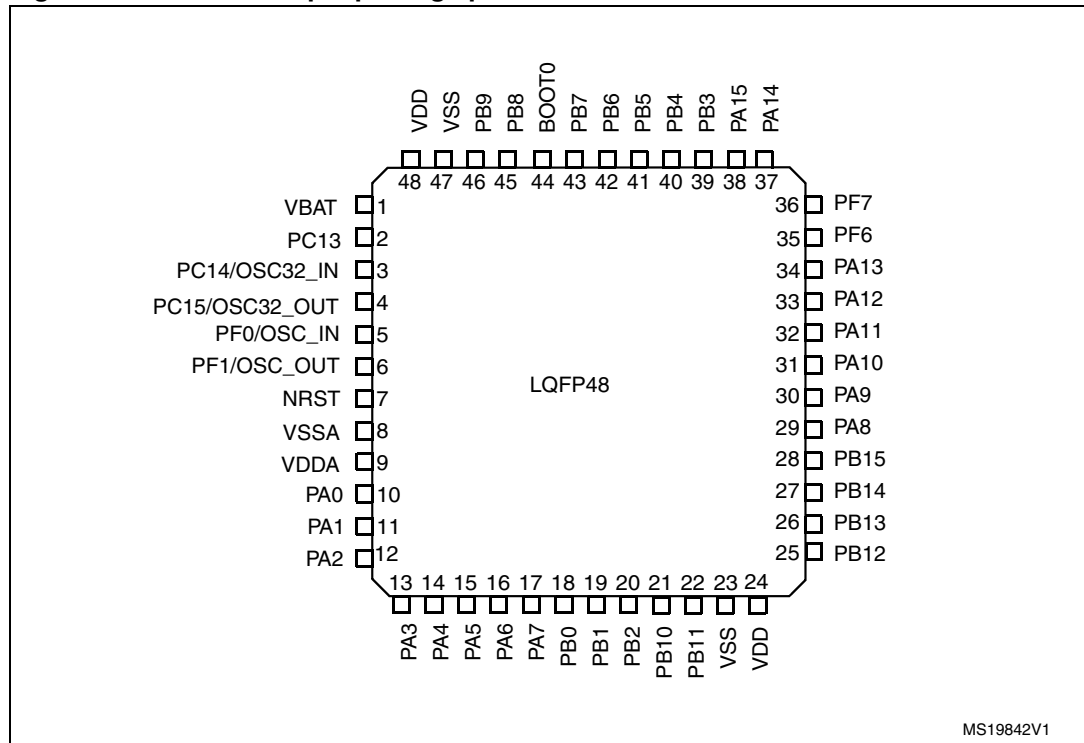
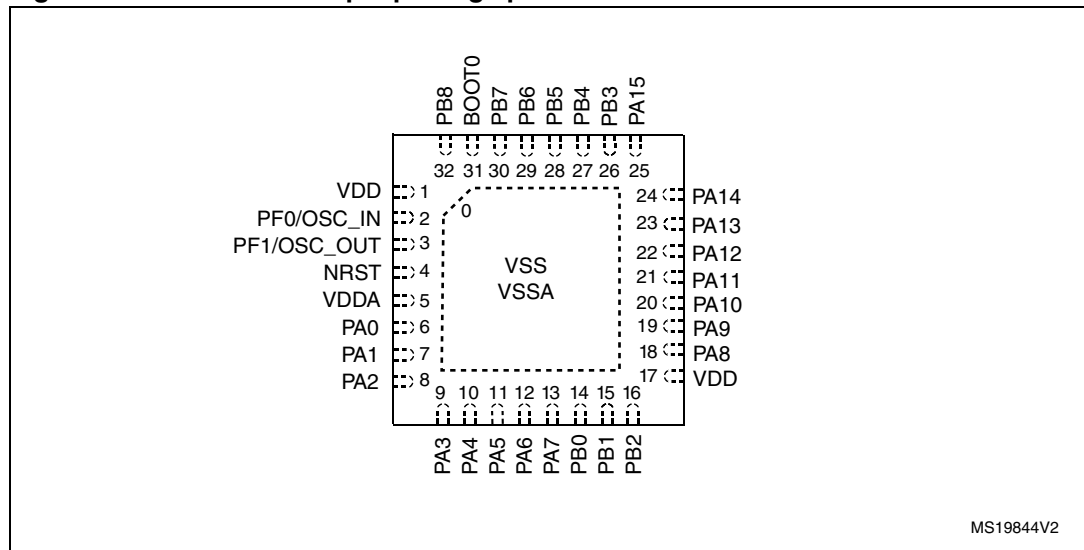


Figure 5. UFQFPN32 32-pin package pinout





**Table 10. Legend/abbreviations used in the pinout table**

| Name          |                      | Abbreviation  | Definition  |
|---------------|----------------------|---|---|
| Pin name      |                      | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name |   |
| Pin type      |                      | S   | Supply pin  |
|               |                      | I   | Input only pin  |
|               |                      | I/O   | Input / output pin  |
| I/O structure |                      | FT  | 5 V tolerant I/O  |
|               |                      | FTf   | 5 V tolerant I/O, FM+ capable                               |
|               |                      | TTa   | 3.3 V tolerant I/O directly connected to ADC                |
|               |                      | TC  | Standard 3.3V I/O   |
|               |                      | B   | Dedicated BOOT0 pin   |
|               |                      | RST   | Bidirectional reset pin with embedded weak pull-up resistor |
| Notes         |                      | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset                                      |   |
| Pin functions | Alternate functions  | Functions selected through GPIOx_AFR registers  |   |
|               | Additional functions | Functions directly selected/enabled through peripheral registers  |   |

**Table 11. Pin definitions**

| Pin number |        |          | Pin name<br>(function after reset) | Pin type | I/O structure | Notes  | Pin functions   |   |
|------------|--------|----------|------------------------------------|----------|---------------|--------|---|---|
| LQFP64     | LQFP48 | UFGFPN32 |                                    |          |               |        | Alternate functions                                     | Additional functions                    |
| 1          | 1      |          | VBAT                               | S        |               |        | Backup power supply                                     |   |
| 2          | 2      |          | PC13                               | I/O      | TC            | (1)(2) |   | RTC_TAMP1,<br>RTC_TS, RTC_OUT,<br>WKUP2 |
| 3          | 3      |          | PC14-OSC32_IN<br>(PC14)            | I/O      | TC            | (1)(2) |   | OSC32_IN                                |
| 4          | 4      |          | PC15-<br>OSC32_OUT<br>(PC15)       | I/O      | TC            | (1)(2) |   | OSC32_OUT                               |
| 5          | 5      | 2        | PF0-OSC_IN<br>(PF0)                | I/O      | FT            |        |   | OSC_IN                                  |
| 6          | 6      | 3        | PF1-OSC_OUT<br>(PF1)               | I/O      | FT            |        |   | OSC_OUT                                 |
| 7          | 7      | 4        | NRST                               | I/O      | RST           |        | Device reset input / internal reset output (active low) |   |

Table 11. Pin definitions (continued)

| Pin number |        |          | Pin name<br>(function after<br>reset) | Pin type | I/O structure | Notes | Pin functions   |  |
|------------|--------|----------|---------------------------------------|----------|---------------|-------|---|--|
| LQFP64     | LQFP48 | UFQFPN32 |                                       |          |               |       | Alternate functions   | Additional functions                               |
| 8          |        |          | PC0                                   | I/O      | TTa           |       | EVENTOUT  | ADC_IN10   |
| 9          |        |          | PC1                                   | I/O      | TTa           |       | EVENTOUT  | ADC_IN11   |
| 10         |        |          | PC2                                   | I/O      | TTa           |       | EVENTOUT  | ADC_IN12   |
| 11         |        |          | PC3                                   | I/O      | TTa           |       | EVENTOUT  | ADC_IN13   |
| 12         | 8      | 0        | VSSA                                  | S        |               |       | Analog ground   |  |
| 13         | 9      | 5        | VDDA                                  | S        |               |       | Analog power supply   |  |
| 14         | 10     | 6        | PA0                                   | I/O      | TTa           |       | USART2_CTS,<br>TIM2_CH1_ETR,<br>COMP1_OUT, TSC_G1_IO1   | ADC_IN0,<br>COMP1_INM6,<br>RTC_TAMP2,<br>WKUP1     |
| 15         | 11     | 7        | PA1                                   | I/O      | TTa           |       | USART2_RTS, TIM2_CH2,<br>TSC_G1_IO2, EVENTOUT   | ADC_IN1,<br>COMP1_INP                              |
| 16         | 12     | 8        | PA2                                   | I/O      | TTa           |       | USART2_TX, TIM2_CH3,<br>TIM15_CH1, COMP2_OUT,<br>TSC_G1_IO3   | ADC_IN2,<br>COMP2_INM6                             |
| 17         | 13     | 9        | PA3                                   | I/O      | TTa           |       | USART2_RX, TIM2_CH4,<br>TIM15_CH2, TSC_G1_IO4   | ADC_IN3,<br>COMP2_INP                              |
| 18         |        |          | PF4                                   | I/O      | FT            |       | EVENTOUT  |  |
| 19         |        |          | PF5                                   | I/O      | FT            |       | EVENTOUT  |  |
| 20         | 14     | 10       | PA4                                   | I/O      | TTa           |       | SPI1_NSS/I2S1_WS,<br>USART2_CK, TIM14_CH1,<br>TSC_G2_IO1  | ADC_IN4,<br>COMP1_INM4,<br>COMP2_INM4,<br>DAC1_OUT |
| 21         | 15     | 11       | PA5                                   | I/O      | TTa           |       | SPI1_SCK/I2S1_CK, CEC,<br>TIM2_CH_ETR, TSC_G2_IO2   | ADC_IN5,<br>COMP1_INM5,<br>COMP2_INM5              |
| 22         | 16     | 12       | PA6                                   | I/O      | TTa           |       | SPI1_MISO/I2S1_MCK,<br>TIM3_CH1, TIM1_BKIN,<br>TIM16_CH1, COMP1_OUT,<br>TSC_G2_IO3, EVENTOUT              | ADC_IN6  |
| 23         | 17     | 13       | PA7                                   | I/O      | TTa           |       | SPI1_MOSI/I2S1_SD,<br>TIM3_CH2, TIM14_CH1,<br>TIM1_CH1N, TIM17_CH1,<br>COMP2_OUT, TSC_G2_IO4,<br>EVENTOUT | ADC_IN7  |
| 24         |        |          | PC4                                   | I/O      | TTa           |       | EVENTOUT  | ADC_IN14   |
| 25         |        |          | PC5                                   | I/O      | TTa           |       | TSC_G3_IO1  | ADC_IN15   |
| 26         | 18     | 14       | PB0                                   | I/O      | TTa           |       | TIM3_CH3, TIM1_CH2N,<br>TSC_G3_IO2, EVENTOUT  | ADC_IN8  |

Table 11. Pin definitions (continued)

| Pin number |        |          | Pin name<br>(function after<br>reset) | Pin type | I/O structure | Notes | Pin functions   |                      |
|------------|--------|----------|---------------------------------------|----------|---------------|-------|---|----------------------|
| LQFP64     | LQFP48 | UFQFPN32 |                                       |          |               |       | Alternate functions   | Additional functions |
| 27         | 19     | 15       | PB1                                   | I/O      | TTa           |       | TIM3_CH4, TIM14_CH1,<br>TIM1_CH3N, TSC_G3_IO3               | ADC_IN9              |
| 28         | 20     | 16       | PB2                                   | I/O      | FT            |       | TSC_G3_IO4  |                      |
| 29         | 21     |          | PB10                                  | I/O      | FT            |       | I2C2_SCL, CEC, TIM2_CH3,<br>TSC_SYNC                        |                      |
| 30         | 22     |          | PB11                                  | I/O      | FT            |       | I2C2_SDA, TIM2_CH4,<br>TSC_G6_IO1, EVENTOUT                 |                      |
| 31         | 23     | 0        | VSS                                   | S        |               |       | Digital ground  |                      |
| 32         | 24     | 17       | VDD                                   | S        |               |       | Digital power supply  |                      |
| 33         | 25     |          | PB12                                  | I/O      | FT            |       | SPI2_NSS, TIM1_BKIN,<br>TSC_G6_IO2, EVENTOUT                |                      |
| 34         | 26     |          | PB13                                  | I/O      | FT            |       | SPI2_SCK, TIM1_CH1N,<br>TSC_G6_IO3                          |                      |
| 35         | 27     |          | PB14                                  | I/O      | FT            |       | SPI2_MISO, TIM1_CH2N,<br>TIM15_CH1, TSC_G6_IO4              |                      |
| 36         | 28     |          | PB15                                  | I/O      | FT            |       | SPI2_MOSI, TIM1_CH3N,<br>TIM15_CH1N, TIM15_CH2              | RTC_REFIN            |
| 37         |        |          | PC6                                   | I/O      | FT            |       | TIM3_CH1  |                      |
| 38         |        |          | PC7                                   | I/O      | FT            |       | TIM3_CH2  |                      |
| 39         |        |          | PC8                                   | I/O      | FT            |       | TIM3_CH3  |                      |
| 40         |        |          | PC9                                   | I/O      | FT            |       | TIM3_CH4  |                      |
| 41         | 29     | 18       | PA8                                   | I/O      | FT            |       | USART1_CK, TIM1_CH1,<br>EVENTOUT, MCO                       |                      |
| 42         | 30     | 19       | PA9                                   | I/O      | FT            |       | USART1_TX, TIM1_CH2,<br>TIM15_BKIN, TSC_G4_IO1              |                      |
| 43         | 31     | 20       | PA10                                  | I/O      | FT            |       | USART1_RX, TIM1_CH3,<br>TIM17_BKIN, TSC_G4_IO2              |                      |
| 44         | 32     | 21       | PA11                                  | I/O      | FT            |       | USART1_CTS, TIM1_CH4,<br>COMP1_OUT, TSC_G4_IO3,<br>EVENTOUT |                      |
| 45         | 33     | 22       | PA12                                  | I/O      | FT            |       | USART1_RTS, TIM1_ETR,<br>COMP2_OUT, TSC_G4_IO4,<br>EVENTOUT |                      |
| 46         | 34     | 23       | PA13<br>(SWDAT)                       | I/O      | FT            | (3)   | IR_OUT, SWDAT   |                      |
| 47         | 35     |          | PF6                                   | I/O      | FT            |       | I2C2_SCL  |                      |
| 48         | 36     |          | PF7                                   | I/O      | FT            |       | I2C2_SDA  |                      |

Table 11. Pin definitions (continued)

| Pin number |        |          | Pin name<br>(function after<br>reset) | Pin type | I/O structure | Notes | Pin functions  |                      |
|------------|--------|----------|---------------------------------------|----------|---------------|-------|--|----------------------|
| LQFP64     | LQFP48 | UFQFPN32 |                                       |          |               |       | Alternate functions                                      | Additional functions |
| 49         | 37     | 24       | PA14<br>(SWCLK)                       | I/O      | FT            | (3)   | USART2_TX, SWCLK   |                      |
| 50         | 38     | 25       | PA15                                  | I/O      | FT            |       | SPI1_NSS/I2S1_WS,<br>USART2_RX, TIM2_CH_ETR,<br>EVENTOUT |                      |
| 51         |        |          | PC10                                  | I/O      | FT            |       |  |                      |
| 52         |        |          | PC11                                  | I/O      | FT            |       |  |                      |
| 53         |        |          | PC12                                  | I/O      | FT            |       |  |                      |
| 54         |        |          | PD2                                   | I/O      | FT            |       | TIM3_ETR   |                      |
| 55         | 39     | 26       | PB3                                   | I/O      | FT            |       | SPI1_SCK/I2S1_CK,<br>TIM2_CH2, TSC_G5_IO1,<br>EVENTOUT   |                      |
| 56         | 40     | 27       | PB4                                   | I/O      | FT            |       | SPI1_MISO/I2S1_MCK,<br>TIM3_CH1, TSC_G5_IO2,<br>EVENTOUT |                      |
| 57         | 41     | 28       | PB5                                   | I/O      | FT            |       | SPI1_MOSI/I2S1_SD,<br>I2C1_SMBA, TIM16_BKIN,<br>TIM3_CH2 |                      |
| 58         | 42     | 29       | PB6                                   | I/O      | FTf           |       | I2C1_SCL, USART1_TX,<br>TIM16_CH1N, TSC_G5_IO3           |                      |
| 59         | 43     | 30       | PB7                                   | I/O      | FTf           |       | I2C1_SDA, USART1_RX,<br>TIM17_CH1N, TSC_G5_IO4           |                      |
| 60         | 44     | 31       | BOOT0                                 | I        | B             |       | Boot memory selection                                    |                      |
| 61         | 45     | 32       | PB8                                   | I/O      | FTf           |       | I2C1_SCL, CEC, TIM16_CH1,<br>TSC_SYNC                    |                      |
| 62         | 46     |          | PB9                                   | I/O      | FTf           |       | I2C1_SDA, IR_OUT,<br>TIM17_CH1, EVENTOUT                 |                      |
| 63         | 47     | 0        | VSS                                   | S        |               |       | Digital ground   |                      |
| 64         | 48     | 1        | VDD                                   | S        |               |       | Digital power supply                                     |                      |

- PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
  - The speed should not exceed 2 MHz with a maximum load of 30 pF
  - these GPIOs must not be used as a current sources (e.g. to drive an LED).
- After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the reference manual.
- After reset, these pins are configured as SWDAT and SWCLK alternate functions, and the internal pull-up on SWDAT pin and internal pull-down on SWCLK pin are activated.


**Table 12. Alternate functions selected through GPIOA\_AFR registers for port A**

| Pin name | AF0                    | AF1        | AF2          | AF3        | AF4       | AF5       | AF6      | AF7       |
|----------|------------------------|------------|--------------|------------|-----------|-----------|----------|-----------|
| PA0      |                        | USART2_CTS | TIM2_CH1_ETR | TSC_G1_IO1 |           |           |          | COMP1_OUT |
| PA1      | EVENTOUT               | USART2_RTS | TIM2_CH2     | TSC_G1_IO2 |           |           |          |           |
| PA2      | TIM15_CH1              | USART2_TX  | TIM2_CH3     | TSC_G1_IO3 |           |           |          | COMP2_OUT |
| PA3      | TIM15_CH2              | USART2_RX  | TIM2_CH4     | TSC_G1_IO4 |           |           |          |           |
| PA4      | SPI1_NSS/<br>I2S1_WS   | USART2_CK  |              | TSC_G2_IO1 | TIM14_CH1 |           |          |           |
| PA5      | SPI1_SCK/<br>I2S1_CK   | CEC        | TIM2_CH1_ETR | TSC_G2_IO2 |           |           |          |           |
| PA6      | SPI1_MISO/<br>I2S1_MCK | TIM3_CH1   | TIM1_BKIN    | TSC_G2_IO3 |           | TIM16_CH1 | EVENTOUT | COMP1_OUT |
| PA7      | SPI1_MOSI/<br>I2S1_SD  | TIM3_CH2   | TIM1_CH1N    | TSC_G2_IO4 | TIM14_CH1 | TIM17_CH1 | EVENTOUT | COMP2_OUT |
| PA8      | MCO                    | USART1_CK  | TIM1_CH1     | EVENTOUT   |           |           |          |           |
| PA9      | TIM15_BKIN             | USART1_TX  | TIM1_CH2     | TSC_G4_IO1 |           |           |          |           |
| PA10     | TIM17_BKIN             | USART1_RX  | TIM1_CH3     | TSC_G4_IO2 |           |           |          |           |
| PA11     | EVENTOUT               | USART1_CTS | TIM1_CH4     | TSC_G4_IO3 |           |           |          | COMP1_OUT |
| PA12     | EVENTOUT               | USART1_RTS | TIM1_ETR     | TSC_G4_IO4 |           |           |          | COMP2_OUT |
| PA13     | SWDAT                  | IR_OUT     |              |            |           |           |          |           |
| PA14     | SWCLK                  | USART2_TX  |              |            |           |           |          |           |
| PA15     | SPI1_NSS/<br>I2S1_WS   | USART2_RX  | TIM2_CH1_ETR | EVENTOUT   |           |           |          |           |

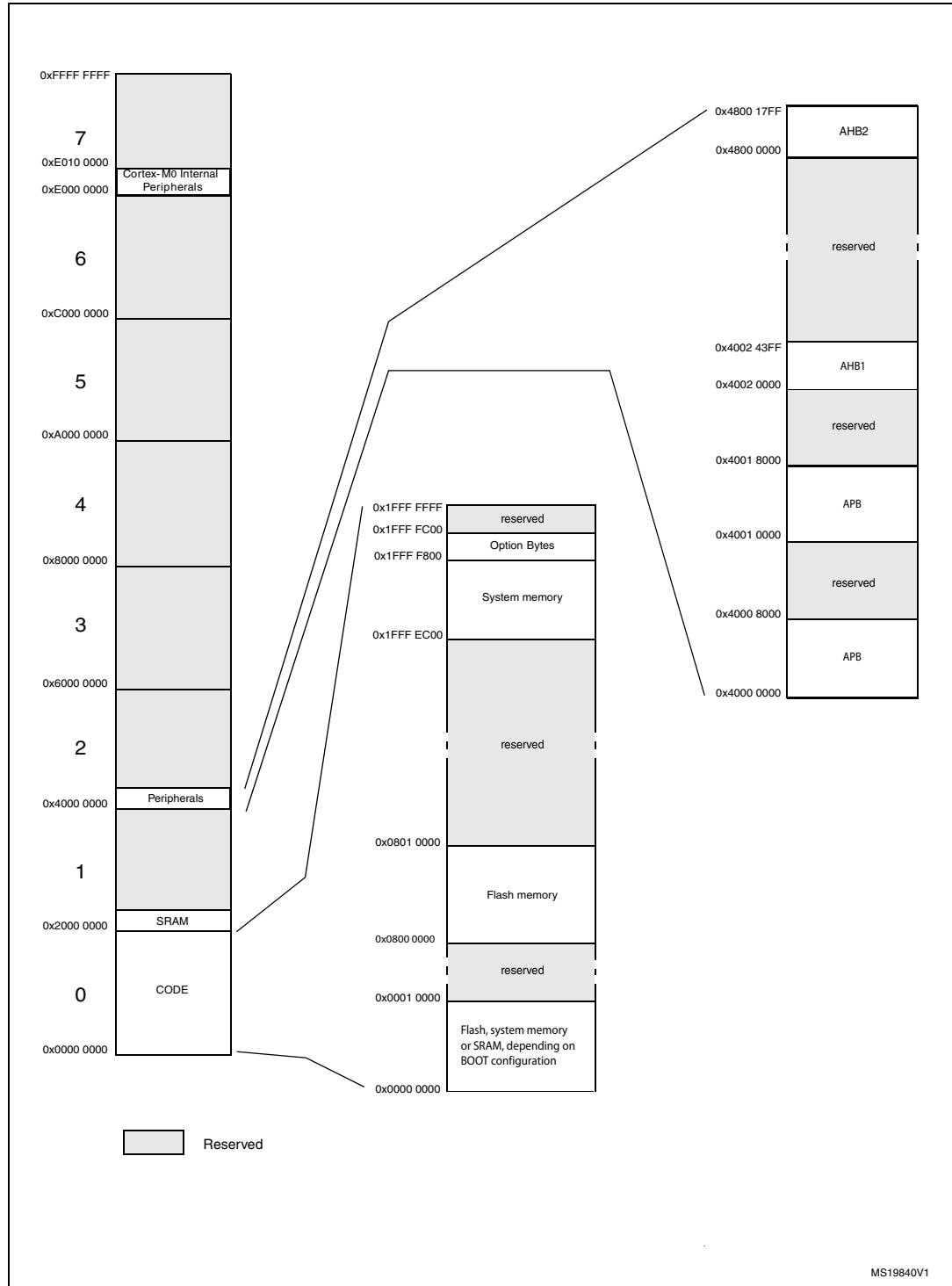


**Table 13. Alternate functions selected through GPIOB\_AFR registers for port B**

| Pin name | AF0                | AF1       | AF2        | AF3        |
|----------|--------------------|-----------|------------|------------|
| PB0      | EVENTOUT           | TIM3_CH3  | TIM1_CH2N  | TSC_G3_IO2 |
| PB1      | TIM14_CH1          | TIM3_CH4  | TIM1_CH3N  | TSC_G3_IO3 |
| PB2      |                    |           |            | TSC_G3_IO4 |
| PB3      | SPI1_SCK/I2S1_CK   | EVENTOUT  | TIM2_CH2   | TSC_G5_IO1 |
| PB4      | SPI1_MISO/I2S1_MCK | TIM3_CH1  | EVENTOUT   | TSC_G5_IO2 |
| PB5      | SPI1_MOSI/I2S1_SD  | TIM3_CH2  | TIM16_BKIN | I2C1_SMBA  |
| PB6      | USART1_TX          | I2C1_SCL  | TIM16_CH1N | TSC_G5_IO3 |
| PB7      | USART1_RX          | I2C1_SDA  | TIM17_CH1N | TSC_G5_IO4 |
| PB8      | CEC                | I2C1_SCL  | TIM16_CH1  | TSC_SYNC   |
| PB9      | IR_OUT             | I2C1_SDA  | TIM17_CH1  | EVENTOUT   |
| PB10     | CEC                | I2C2_SCL  | TIM2_CH3   | TSC_SYNC   |
| PB11     | EVENTOUT           | I2C2_SDA  | TIM2_CH4   | TSC_G6_IO1 |
| PB12     | SPI2_NSS           | EVENTOUT  | TIM1_BKIN  | TSC_G6_IO2 |
| PB13     | SPI2_SCK           |           | TIM1_CH1N  | TSC_G6_IO3 |
| PB14     | SPI2_MISO          | TIM15_CH1 | TIM1_CH2N  | TSC_G6_IO4 |
| PB15     | SPI2_MOSI          | TIM15_CH2 | TIM1_CH3N  | TIM15_CH1N |

# 5 Memory mapping

Figure 6. STM32F051x memory map



MS19840V1

Table 14. STM32F051x peripheral register boundary addresses

| Bus                       | Boundary address          | Size          | Peripheral      |
|---------------------------|---------------------------|---------------|-----------------|
|                           | 0x4800 1800 - 0x5FFF FFFF | ~384 MB       | Reserved        |
| AHB2                      | 0x4800 1400 - 0x4800 17FF | 1KB           | GPIOF           |
|                           | 0x4800 1000 - 0x4800 13FF | 1KB           | Reserved        |
|                           | 0x4800 0C00 - 0x4800 0FFF | 1KB           | GPIOD           |
|                           | 0x4800 0800 - 0x4800 0BFF | 1KB           | GPIOC           |
|                           | 0x4800 0400 - 0x4800 07FF | 1KB           | GPIOB           |
|                           | 0x4800 0000 - 0x4800 03FF | 1KB           | GPIOA           |
|                           | 0x4002 4400 - 0x47FF FFFF | ~128 MB       | Reserved        |
| AHB1                      | 0x4002 4000 - 0x4002 43FF | 1KB           | TSC             |
|                           | 0x4002 3400 - 0x4002 3FFF | 3KB           | Reserved        |
|                           | 0x4002 3000 - 0x4002 33FF | 1KB           | CRC             |
|                           | 0x4002 2400 - 0x4002 2FFF | 3KB           | Reserved        |
|                           | 0x4002 2000 - 0x4002 23FF | 1KB           | FLASH Interface |
|                           | 0x4002 1400 - 0x4002 1FFF | 3KB           | Reserved        |
|                           | 0x4002 1000 - 0x4002 13FF | 1KB           | RCC             |
|                           | 0x4002 0400 - 0x4002 0FFF | 3KB           | Reserved        |
|                           | 0x4002 0000 - 0x4002 03FF | 1KB           | DMA             |
|                           | 0x4001 8000 - 0x4001 FFFF | 32KB          | Reserved        |
| APB                       | 0x4001 5C00 - 0x4001 7FFF | 9KB           | Reserved        |
|                           | 0x4001 5800 - 0x4001 5BFF | 1KB           | DBGMCU          |
|                           | 0x4001 4C00 - 0x4001 57FF | 3KB           | Reserved        |
|                           | 0x4001 4800 - 0x4001 4BFF | 1KB           | TIM17           |
|                           | 0x4001 4400 - 0x4001 47FF | 1KB           | TIM16           |
|                           | 0x4001 4000 - 0x4001 43FF | 1KB           | TIM15           |
|                           | 0x4001 3C00 - 0x4001 3FFF | 1KB           | Reserved        |
|                           | 0x4001 3800 - 0x4001 3BFF | 1KB           | USART1          |
|                           | 0x4001 3400 - 0x4001 37FF | 1KB           | Reserved        |
|                           | 0x4001 3000 - 0x4001 33FF | 1KB           | SPI1/I2S1       |
|                           | 0x4001 2C00 - 0x4001 2FFF | 1KB           | TIM1            |
|                           | 0x4001 2800 - 0x4001 2BFF | 1KB           | Reserved        |
|                           | 0x4001 2400 - 0x4001 27FF | 1KB           | ADC             |
|                           | 0x4001 0800 - 0x4001 23FF | 7KB           | Reserved        |
|                           | 0x4001 0400 - 0x4001 07FF | 1KB           | EXTI            |
| 0x4001 0000 - 0x4001 03FF | 1KB                       | SYSCFG + COMP |                 |
|                           | 0x4000 8000 - 0x4000 FFFF | 32KB          | Reserved        |



**Table 14. STM32F051x peripheral register boundary addresses (continued)**

| Bus                       | Boundary address          | Size | Peripheral |
|---------------------------|---------------------------|------|------------|
| APB                       | 0x4000 7C00 - 0x4000 7FFF | 1KB  | Reserved   |
|                           | 0x4000 7800 - 0x4000 7BFF | 1KB  | CEC        |
|                           | 0x4000 7400 - 0x4000 77FF | 1KB  | DAC        |
|                           | 0x4000 7000 - 0x4000 73FF | 1KB  | PWR        |
|                           | 0x4000 5C00 - 0x4000 6FFF | 5KB  | Reserved   |
|                           | 0x4000 5800 - 0x4000 5BFF | 1KB  | I2C2       |
|                           | 0x4000 5400 - 0x4000 57FF | 1KB  | I2C1       |
|                           | 0x4000 4800 - 0x4000 53FF | 3 KB | Reserved   |
|                           | 0x4000 4400 - 0x4000 47FF | 1KB  | USART2     |
|                           | 0x4000 3C00 - 0x4000 43FF | 2KB  | Reserved   |
|                           | 0x4000 3800 - 0x4000 3BFF | 1KB  | SPI2       |
|                           | 0x4000 3400 - 0x4000 37FF | 1KB  | Reserved   |
|                           | 0x4000 3000 - 0x4000 33FF | 1KB  | IWWDG      |
|                           | 0x4000 2C00 - 0x4000 2FFF | 1KB  | WWDG       |
|                           | 0x4000 2800 - 0x4000 2BFF | 1KB  | RTC        |
|                           | 0x4000 2400 - 0x4000 27FF | 1KB  | Reserved   |
|                           | 0x4000 2000 - 0x4000 23FF | 1KB  | TIM14      |
|                           | 0x4000 1400 - 0x4000 1FFF | 3KB  | Reserved   |
|                           | 0x4000 1000 - 0x4000 13FF | 1KB  | TIM6       |
|                           | 0x4000 0800 - 0x4000 0FFF | 2KB  | Reserved   |
| 0x4000 0400 - 0x4000 07FF | 1KB                       | TIM3 |            |
| 0x4000 0000 - 0x4000 03FF | 1KB                       | TIM2 |            |

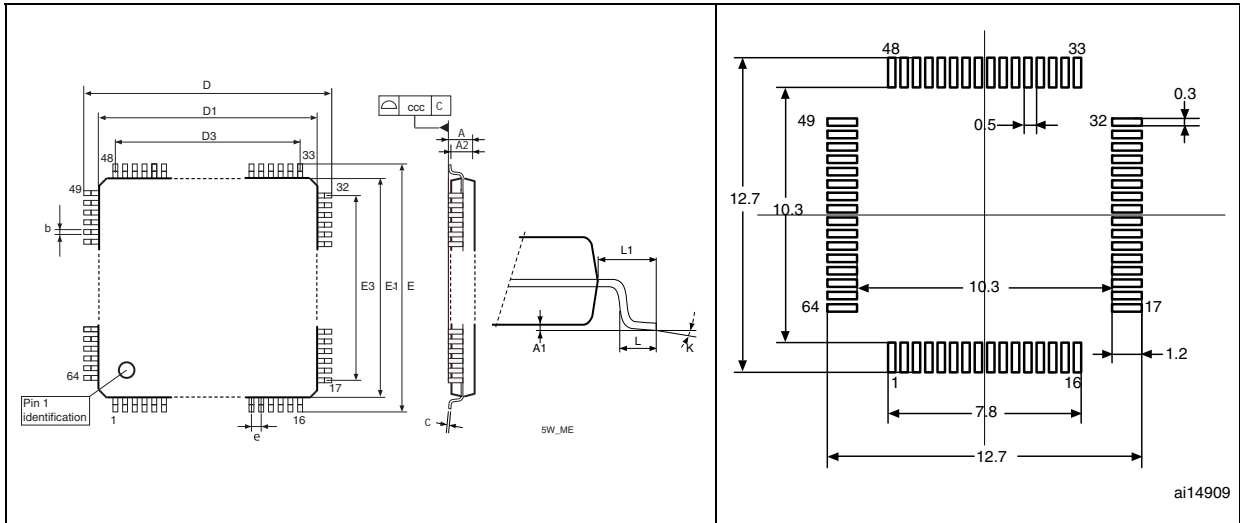
## 6 Package characteristics

### 6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 7. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline<sup>(1)</sup>

Figure 8. Recommended footprint<sup>(1)(2)</sup>



1. Drawing is not to scale.
2. Dimensions are in millimeters.

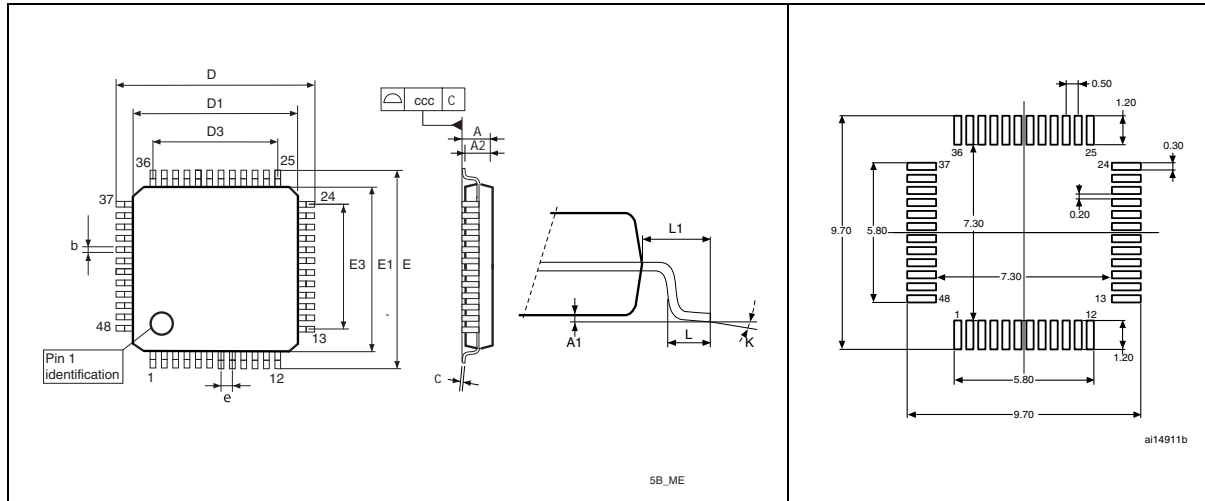
Table 15. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

| Symbol | millimeters           |        |        | inches <sup>(1)</sup> |        |        |
|--------|-----------------------|--------|--------|-----------------------|--------|--------|
|        | Min                   | Typ    | Max    | Min                   | Typ    | Max    |
| A      |                       |        | 1.600  |                       |        | 0.0630 |
| A1     | 0.050                 |        | 0.150  | 0.0020                |        | 0.0059 |
| A2     | 1.350                 | 1.400  | 1.450  | 0.0531                | 0.0551 | 0.0571 |
| b      | 0.170                 | 0.220  | 0.270  | 0.0067                | 0.0087 | 0.0106 |
| c      | 0.090                 |        | 0.200  | 0.0035                |        | 0.0079 |
| D      | 11.800                | 12.000 | 12.200 | 0.4646                | 0.4724 | 0.4803 |
| D1     | 9.800                 | 10.000 | 10.200 | 0.3858                | 0.3937 | 0.4016 |
| D.     |                       | 7.500  |        |                       |        |        |
| E      | 11.800                | 12.000 | 12.200 | 0.4646                | 0.4724 | 0.4803 |
| E1     | 9.800                 | 10.00  | 10.200 | 0.3858                | 0.3937 | 0.4016 |
| e      |                       | 0.500  |        |                       | 0.0197 |        |
| k      | 0°                    | 3.5°   | 7°     | 0°                    | 3.5°   | 7°     |
| L      | 0.450                 | 0.600  | 0.75   | 0.0177                | 0.0236 | 0.0295 |
| L1     |                       | 1.000  |        |                       | 0.0394 |        |
| ccc    |                       | 0.080  |        |                       | 0.0031 |        |
| N      | <b>Number of pins</b> |        |        |                       |        |        |
|        | 64                    |        |        |                       |        |        |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 9. LQFP48 – 7 x 7mm, 48-pin low-profile quad flat package outline<sup>(1)</sup>

Figure 10. Recommended footprint<sup>(1)(2)</sup>



1. Drawing is not to scale.
2. Dimensions are in millimeters.

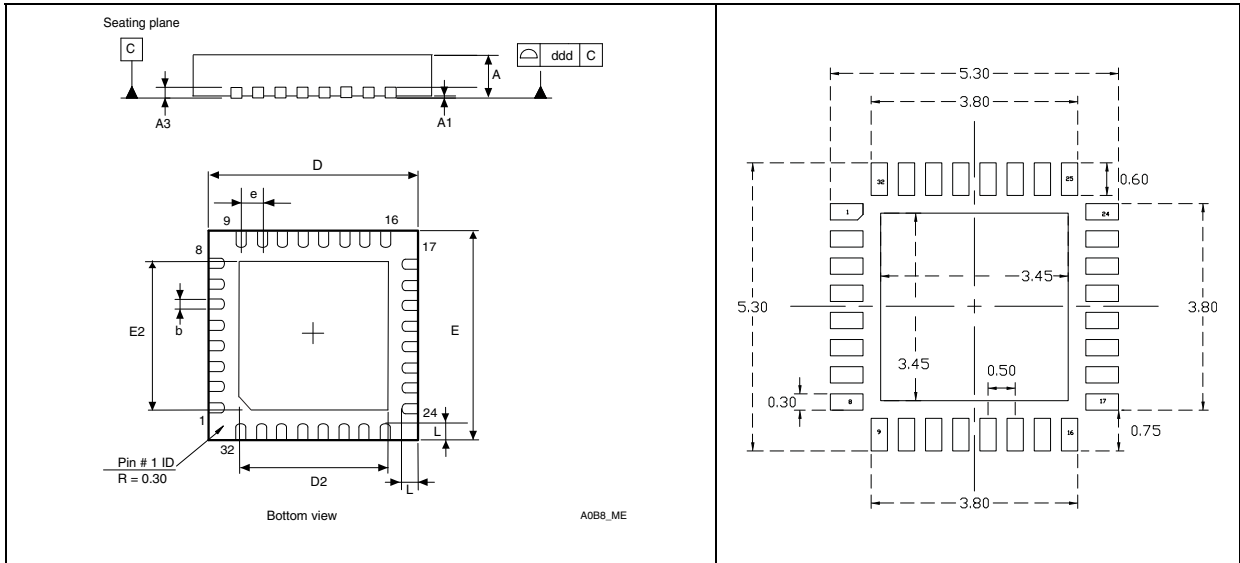
Table 16. LQFP48 – 7 x 7mm, 48-pin low-profile quad flat package mechanical data

| Symbol | millimeters |       |       | inches <sup>(1)</sup> |        |        |
|--------|-------------|-------|-------|-----------------------|--------|--------|
|        | Min         | Typ   | Max   | Min                   | Typ    | Max    |
| A      |             |       | 1.600 |                       |        | 0.0630 |
| A1     | 0.050       |       | 0.150 | 0.0020                |        | 0.0059 |
| A2     | 1.350       | 1.400 | 1.450 | 0.0531                | 0.0551 | 0.0571 |
| b      | 0.170       | 0.220 | 0.270 | 0.0067                | 0.0087 | 0.0106 |
| c      | 0.090       |       | 0.200 | 0.0035                |        | 0.0079 |
| D      | 8.800       | 9.000 | 9.200 | 0.3465                | 0.3543 | 0.3622 |
| D1     | 6.800       | 7.000 | 7.200 | 0.2677                | 0.2756 | 0.2835 |
| D3     |             | 5.500 |       |                       | 0.2165 |        |
| E      | 8.800       | 9.000 | 9.200 | 0.3465                | 0.3543 | 0.3622 |
| E1     | 6.800       | 7.000 | 7.200 | 0.2677                | 0.2756 | 0.2835 |
| E3     |             | 5.500 |       |                       | 0.2165 |        |
| e      |             | 0.500 |       |                       | 0.0197 |        |
| L      | 0.450       | 0.600 | 0.750 | 0.0177                | 0.0236 | 0.0295 |
| L1     |             | 1.000 |       |                       | 0.0394 |        |
| k      | 0°          | 3.5°  | 7°    | 0°                    | 3.5°   | 7°     |
| ccc    |             | 0.080 |       |                       | 0.0031 |        |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 11. UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package outline (5 x 5)<sup>(1)(2)(3)</sup>**

**Figure 12. UFQFPN32 recommended footprint<sup>(1)(4)</sup>**



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. This pad is used for the device ground and must be connected. It is referred to as pin 0 in [Table 11: Pin definitions](#).
4. Dimensions are in millimeters.

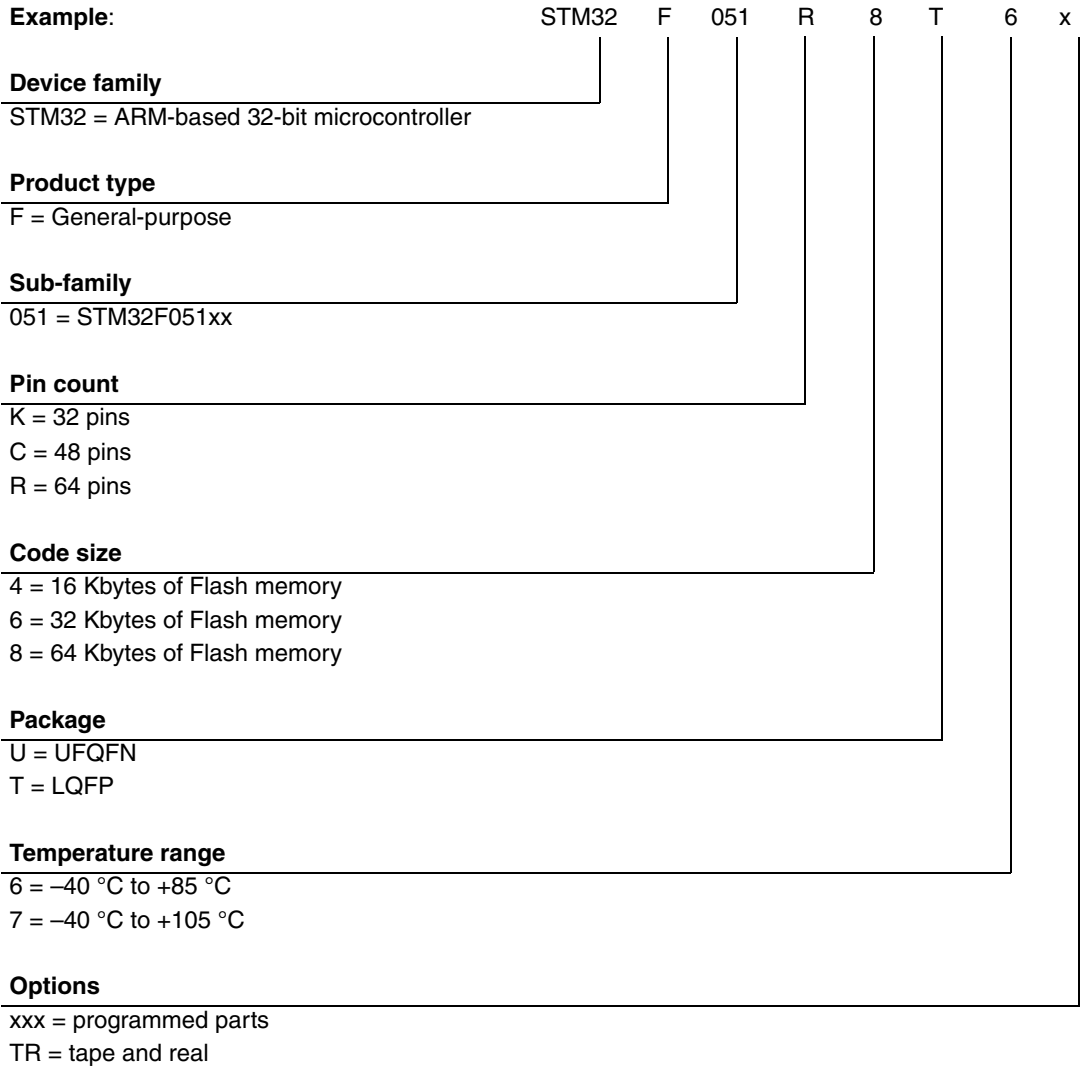
**Table 17. UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package (5 x 5), package mechanical data**

| Dim. | mm             |       |      | inches <sup>(1)</sup> |        |        |
|------|----------------|-------|------|-----------------------|--------|--------|
|      | Min            | Typ   | Max  | Min                   | Typ    | Max    |
| A    | 0.5            | 0.55  | 0.6  | 0.0197                | 0.0217 | 0.0236 |
| A1   | 0.00           | 0.02  | 0.05 | 0                     | 0.0008 | 0.0020 |
| A3   |                | 0.152 |      |                       | 0.006  |        |
| b    | 0.18           | 0.23  | 0.28 | 0.0071                | 0.0091 | 0.0110 |
| D    | 4.90           | 5.00  | 5.10 | 0.1929                | 0.1969 | 0.2008 |
| D2   |                | 3.50  |      |                       | 0.1378 |        |
| E    | 4.90           | 5.00  | 5.10 | 0.1929                | 0.1969 | 0.2008 |
| E2   | 3.40           | 3.50  | 3.60 | 0.1339                | 0.1378 | 0.1417 |
| e    |                | 0.500 |      |                       | 0.0197 |        |
| L    | 0.30           | 0.40  | 0.50 | 0.0118                | 0.0157 | 0.0197 |
| ddd  |                | 0.08  |      |                       | 0.0031 |        |
|      | Number of pins |       |      |                       |        |        |
| N    | 32             |       |      |                       |        |        |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

# 7 Ordering information scheme

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.



## 8 Revision history

**Table 18. Document revision history**

| Date        | Revision | Changes   |
|-------------|----------|---|
| 09-Feb-2012 | 1        | Initial release   |
| 14-Feb-2012 | 2        | Added <a href="#">Table 2: STM32F051xx family device features and peripheral counts</a><br>Updated <a href="#">Table 7: STM32F051x SPI/I2S implementation</a> |

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